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Date 8/12/02 Serial # 09/853,089 Priority Application Date 3/19/01

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What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining th desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe t topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-28

Problem: See Page 1 lines 21-34

Solution: " " 9 " 1-17

novelty in structure illustrated in the claims

Staff Use Only	Type of Search	Vendors
Searcher: Irina Speckhard	Structure (#)_____	STN ✓
Searcher Phone: 308-6559	Bibliographic ✓	Dialog ✓
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation_____	Questel/Orbit_____
Date Searcher Picked Up: 8/13/02	Fulltext ✓	Lexis-Nexis_____
Date Completed: 8/13/02	Patent Family_____	WWW/Internet_____
Searcher Prep/Rev Time: 100	Other_____	Other_____
Online Time: 180		

08/13/2002 09/813,087

13aug02 15:40:42 User267149 Session D278.1

SYSTEM:OS - DIALOG OneSearch
File 348:EUROPEAN PATENTS 1978-2002/Aug W01
(c) 2002 European Patent Office
File 349:PCT FULLTEXT 1983-2002/UB=20020808,UT=20020801
(c) 2002 WIPO/Univentio

```
Set     Items   Description
S1      10672   (MOS OR METAL()OXIDE(1W)SEMICONDUCT??????? OR NMOS? ?  OR -
             N()MOS? ? OR PMOS? ? OR P()MOS? ? OR VMOS? ? OR V()MOS? ? OR -
             CMOS? ? OR C()MOS? ?)/TI,AB,CM
S2       3582   (MOSFET? ? OR MOS()FET? ? OR METAL()OXIDE(1W)SEMICONDUCT??-
             ???)/TI,AB,CM
S3       7638   ((FIELD()EFFECT? ?(1W)TRANSIST???????) OR FET)/TI,AB,CM
S4      18101   S1:S3
S5     345334   (CIRCUIT?????? OR LOOP? ? OR PATH? ? OR ROUTE? ? OR ELECTR-
             ODE? ?)/TI,AB,CM
S6      22867   (INTEGRAT??????(3N)(CIRCUIT?????? OR LOOP? ?))/TI,AB,CM
S7     345334   S5:S6
S8       4720   (PRINTHEAD? ? OR PRINT()HEAD? ?)/TI,AB,CM
S9       1423   ((FLUID? ? OR LIQUID? ?)()JET? ?  OR FLUIDJET? ?)/TI,AB,CM
S10      9219   (INKJET? ? OR INK()JET? ? OR INK()JETT??? OR INKJETT???)/T-
             I,AB,CM
S11     10540   S9:S10
S12    106411   SUBSTRATE? ?/TI,AB,CM
S13     30168   TRANSISTOR? ?/TI,AB,CM
S14       908   ((FLUID? ? OR LIQUID? ?)(3N)(CARRIAGE? ?  OR CARTRIDGE? ?)-
             )/TI,AB,CM
S15      7049   (RECORD??????(3N)DEVICE? ?)/TI,AB,CM
S16     29956   ((PRESSUR?????? OR COMPRESS??????)(3N)(REGULAT?????? OR CO-
             NTROL?????? OR DIRECT??????))/TI,AB,CM
S17     20841   (AIR(3N)(PRESSUR?????? OR COMPRESS??????))/TI,AB,CM
S18     46260   S16:S17
S19       711   (EJECT??????(3N)ELEMENT? ?)/TI,AB,CM
S20   1044294   ((SILICON()DIOXIDE) OR SI02 OR QUARTZ OR (SILICON()NITRIDE)
              OR SIN OR (SILICON()CARBIDE) OR CARBOLON OR CARBORUNDUM OR T-
             ANTALUM OR TA OR ALUMINIUM  OR ALUMINUM OR AL OR COPPER OR CU
             OR GOLD OR AUTUNGSTEN OR MOLYBDENUM OR MO)/TI,AB,CM
S21     13936   S4 AND S7
S22      9983   S21 AND S20
S23        43   S22 AND S8
S24        30   S23 AND S11
S25        24   S24 AND S12
S26         0   S25 AND S14
S27         1   S25 AND (CARRIAGE? ?  OR CARTRIDGE? ?)/TI,AB,CM
S28        23   S25 NOT S27
S29         0   S28 AND S15
S30         1   S28 AND S18
S31        22   S28 NOT S30
S32         1   S31 AND S19
S33        21   S31 NOT S32
S34        17   S33 AND S1
S35        10   S34 AND S6
S36        10   S35 AND PRINT???????/TI,AB,CM
S37        10   S36 AND S10
S38        10   IDPAT (sorted in duplicate/non-duplicate order)
S39        10   IDPAT (primary/non-duplicate records only)
S40      3244   S20 AND S8
S41        38   S40 AND S1
S42         0   S41 AND S9
```

S43	27	S41 AND S10
S44	0	S43 AND S15
S45	2	S43 AND S19
S46	25	S43 NOT S45
S47	17	*deleted* S46 AND S13
S48	17	S46 AND S13
S49	0	S48 AND S15
S50	0	S48 AND S18
S51	8	S48 AND EJECT??????/TI,AB,CM
S52	8	IDPAT (sorted in duplicate/non-duplicate order)
S53	8	IDPAT (primary/non-duplicate records only)

08/13/2002 09/813,087

27/TI,PN,PY,PD,K/1 (Item 1 from file: 349)
DIALOG(R)File 349:(c) 2002 WIPO/Univentio. All rts. reserv.

ALIGNING METHOD FOR MULTIPLE **INK JET** COLOUR **PRINTHEADS** WITH BUILT-IN OPTOELECTRONIC POSITION DETECTOR
PROCEDE D'ALIGNEMENT DE PLUSIEURS TETES D'IMPRIMANTE COULEUR A JET D'ENCRE, A L'AIDE D'UN CAPTEUR DE POSITION OPTOELECTRONIQUE INTEGRE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200058101 A1 20001005 (WO 0058101)
Publication Year: 2000

English Abstract
The single heads (40) mounted on a single print **carriage** of an **ink jet** printer comprise a column (50) of phototransistors (51-i), built directly into the chip of each head in the same process steps as used for the **circuits** for selecting and driving the actuating resistors; an illuminating device (43) on board the printer focuses a light spot (70) on the column (50) of...

23 **Ink jet** dot-matrix **printhead** comprising:
a semiconductor **substrate**;
a first plurality of ejection elements integrated on said **substrate**, for the generation of droplets of ink through a corresponding plurality of nozzles, arranged at a constant pitch in at least one row according to a first vertical
direction;
a second plurality of electronic components integrated on said **substrate**
by means of a **C-MOS** technology for selecting and driving said first plurality of
ejection elements,
characterized in that it further comprises a column (50) made up of a plurality of phototransistors (5 I-i) integrated on said **substrate** by means of said **C-MOS** technol

...currents (1-i) which are scanned in sequence (K) times, 'in order to generate a unique signal (V-i) on a video output (57).
30 **Ink jet** dot-matrix **printhead** comprising:
1 5 - a semiconductor **substrate**;

185. A method as claUned in claim 184 wherein said integrated drive electronics comprise a **CMOS** process. 186. A method as claiined in claim 180 wherein ink is ejected from said **substrate** substantially non'nal to said **substrate**. 187. A method of manufacture of an **ink jet print head** arrangement including a series of nozzle chambers, said method comprising the steps of-. (a) utilizing an initial semiconductor wafer having an electrical **circuitry** layer fon-ned thereon
on;
(b) fortning a bottorn **electrode** layer of conductive material on or in said electrical **circuitry**
io layer;

32/TI,PN,PY,PD,K/1 (Item 1 from file: 348)

Ink-jet element **substrate, ink-jet** printing head and **ink-jet** printing apparatus
Substrat fur ein Element eines Tintenstrahldruckkopfes, Tintenstrahldruckkopf und Tintenstrahldruckapparat
Substrat pour element a jet d'encre, tete d'impression a jet d'encre et appareil d'impression a jet d'encre
PATENT (CC, No, Kind, Date): EP 805029 A2 971105 (Basic)
EP 805029 A3 980624
EP 805029 B1 020320

Employing a multi-value heater which can obtain high level gradation, a **circuit** construction can be simplified, and compact head can be realized. Therefore, corresponding to a plurality of ejection openings, a plurality of heating elements (201(1)... 201(n)) are provided corresponding thereto. The heating elements (201(1)... 201(n)) are supplied selection **signal** so as to be driven selectively.

CLAIMS 1. A **substrate** for an **ink-jet** element of an **ink-jet** printing head ejecting an ink through a plurality of ejection openings, characterized by comprising:
a plurality of heating elements provided for each of said plurality of ejection openings and generating a **thermal** energy for ejecting th

10. A **substrate** for an **ink-jet** element as set forth in claim 1, characterized in that said driving **circuit** includes a **N-MOS** transistor.

11. A **substrate** for an **ink-jet** element as set forth in claim 1, characterized in that said selection **circuit** is a **circuit** for supplying a selection **signal** corresponding to respective of said plurality of heating elements per each of said ejection openings.

45. An **ink-jet** printing apparatus as set forth in claim 31, characterized in that said heating element is an **electrothermal** transducer.

46. A **substrate** for an **ink jet** recording head or an **ink jet** recording head or an apparatus having at least one **ink jet** recording head comprising such a **substrate**, wherein the **substrate** comprises heating **elements** for causing ink **ejection**, means for driving the heating elements, and/or means for holding image data and/or means for selecting a heating element to be driven.

...CLAIMS B1

1. A **substrate** for an **ink jet print head** for ejecting ink through a plurality of ejection openings, the **substrate** comprising:
a selection **circuit** (307) for receiving from the data holding **circuit** (303) the image data to be recorded by each of the ejection openings and for selecting for each ejection opening one or more of the plurality of heating **elements** associated with that **ejection** opening to be driven; and

08/13/2002 09/813,087

39/TI,PN,PD,PY,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Incorporation of supplementary heaters in the ink channels of **cmos** /mems integrated **ink jet print head** and method of forming same
PATENT (CC, No, Kind, Date): EP 1219427 A2 020703 (Basic)

An **ink jet print head** is formed of a silicon **substrate** that includes **integrated circuits** formed therein for controlling operation of the **print head**. The silicon **substrate** has a series of ink channels formed therein along the length of the **substrate**. An insulating layer or layers overlying the silicon **substrate** has a series of nozzle openings or bores formed therein along the length of the **substrate** and each nozzle bore communicates with a respective ink channel. A primary heater element is associated with each nozzle bore for asymmetrically heating the ink...

2. The **ink jet print head** of claim 1 wherein the insulating layer or layers includes a series of vertically separated levels of electrically conductive leads and electrically conductive vias connect at least some of said levels.
5. The **ink jet print head** of any of claims 1 through 4 wherein the **integrated circuits** include **CMOS** devices.
9. The method of claim 8 and wherein the **integrated circuits** include **CMOS** devices that are used to control the primary heater element formed adjacent the nozzle bore.
10. The method of claim 9 and wherein an insulating layer or layers is supported on the silicon **substrate** and the insulating layer or layers includes a series of vertically separated levels of electrically conductive leads and electrically conductive vias connect at least some of the levels and signals are transmitted from the **CMOS** devices formed in the **substrate** through the electrically conductive vias to the primary heater element.

39/TI,PN,PD,PY,K/3 (Item 3 from file: 348)

Cmos/mems integrated **ink jet print head** with oxide based **lateral** flow nozzle architecture and method of forming same
Cmos/mems integrierter Tintenstrahldruckkopf mit Querflussdusenarchitektur auf Oxidbasis und Verfahren zu seiner Herstellung
Tete d'impression a jet d'encre integree **Cmos** /mems avec une architecture de buse a flux **lateral** a base d'oxide et methode de fabrication
PATENT (CC, No, Kind, Date): EP 1219425 A2 020703 (Basic)

A continuous **ink jet print head** is formed using a combination of **traditional CMOS** technology to form the various controlling **electrical circuits** on a silicon **substrate** having insulating layer(s) which provide **electrical** connections and a MEMS technology for forming nozzle openings. A blocking structure is formed in the insulating layer(s) between a first ink channel formed in the silicon **substrate** and a second ink channel formed in the insulating layer(s). The blocking structure causes ink to flow around the blocking structure and thereby develop **lateral** flow components to the liquid entering the second channel so that, for droplets selected for **printing**, as the stream of droplets emanates from the bore of the nozzle, there is provided a reduced amount of heat needed for operating a heating...

...CLAIMS A2
1. A continuous **ink jet print head** having a plurality of nozzles, the **print head** comprising:
a silicon **substrate** including **integrated circuits** formed therein for controlling operation of the **print head**, the silicon **substrate** having a primary ink channel formed therein;
an insulating layer or layers supported on the silicon **substrate**

...ink channel to flow about the blocking structure and to enter the secondary ink channel at a location offset from the nozzle bore to provide **lateral** flow components to the liquid ink entering the nozzle bore.
8. The **print head** of any of claims 1 through 7 wherein the **integrated circuits** include **CMOS** devices.
9. A method of operating a continuous **ink jet print head** having a plurality of nozzles with each nozzle having a nozzle bore, the method comprising:
providing liquid ink under pressure in a primary ink channel formed in a silicon **substrate** having a series of **integrated circuits** formed therein for controlling operation of the **print head**

08/13/2002 09/813,087

39/TI,PN,PD,PY,K/4 (Item 4 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Cmos/mems integrated **ink jet print head** with silicon based **lateral** flow nozzle architecture and method of forming same
Cmos/mems integrierter Tintenstrahldruckkopf mit Querflussdusenarchitektur auf Siliziumbasis und Verfahren zu seiner Herstellung
Tete d'impression a jet d'encre integree **Cmos** /mems avec une architecture de buse a flux **lateral** a base de silicone et methode de fabrication
PATENT (CC, No, Kind, Date): EP 1219424 A2 020703 (Basic)

A continuous **ink jet print head** is formed using a combination of **traditional CMOS** technology to form the various controlling **electrical circuits** on a silicon **substrate** having insulating layer(s) which provide **electrical** connections to heater elements associated with a nozzle and a MEMS technology for forming ink delivery cavities or channels and bores. A blocking structure is formed in the silicon **substrate** between an ink channel formed in the silicon **substrate** and a nozzle bore formed in the insulating layer(s). The blocking structure causes ink in an ink channel to flow around the blocking structure and thereby develop **lateral** flow components to the liquid entering the bore so that as the stream of fluid emanates from the bore the **lateral** flow components are a factor in allowing an increased stream deflection under the condition of asymmetric heating.

...CLAIMS A2
1. A continuous **ink jet print head** having a plurality of nozzles, the **print head** comprising:
a silicon **substrate** including **integrated circuits** formed therein for controlling operation of the **print head**, the silicon **substrate** having an ink channel formed therein;
communicate with the bore; and
forming a blocking structure in the silicon **substrate** for controlling **lateral** flow of ink from the ink channel formed in the silicon **substrate** to the bore formed in the insulating layer or layers.

08/13/2002 09/813,087

39/TI,PN,PD,PY,K/5 (Item 5 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Incorporation of silicon bridges in the ink channels of **cmos**/mems integrated **ink jet print head** and method of forming same
Einbauen von Silizium Brucken in Tintenkanale eines **Cmos** /Mems integrierten Tintenstrahldruckkopfs und dazugehoriges Herstellungsverfahren
Incorportation de ponts de silicium dans les canaux d'encre d'une tete jet d'encre integree **cmos**/mems et procede de fabrication
PATENT (CC, No, Kind, Date): EP 1219422 A1 020703 (Basic)

An **ink jet print head** is formed of a silicon **substrate** that includes **integrated circuits** formed therein for controlling operation of the **print head**. The silicon **substrate** has a series of ink channels formed therein along the **longitudinal** direction of the nozzle array. An insulating layer or layers overlying the silicon **substrate** has a series or an array of nozzle openings or bores formed therein along the length of the **substrate** and each nozzle opening communicates with a respective ink channel. A series of rib structures is formed in the silicon **substrate** transverse to the **longitudinal** direction of the nozzle array for providing strength to the **final** silicon ship comprising the **print head**.

1. An **ink jet print head** comprising:
   a silicon **substrate** including **integrated circuits** formed therein for controlling operation of the **print head**, the silicon **substrate** having a series of ink channels formed therein along the length of the **substrate**;
   an insulating layer or layers overlying the silicon **substrate**, the insulating layer or layers having a series of **ink jet** bores formed therein along the length of the **substrate** and each bore communicates with an ink channel; and
   a series of ribbed structures formed in the silicon **substrate** transverse to the length of the **substrate** for providing strength to the **substrate**.

5. The **ink jet print head** of any of claims 1 through 4 wherein the **integrated circuits** include **CMOS** devices.

10. A method of forming an **ink jet print head** comprising:
   providing a silicon **substrate** having **integrated circuits** for controlling operation of the **print head**, the silicon **substrate** having an insulating layer or layers formed thereon, the insulating layer or layers having **electrical** conductors formed therein that are electrically connected to **circuits** formed in the silicon **substrat**

08/13/2002 09/813,087

9/TI,PN,PD,PY,K/6 (Item 6 from file: 348)
DIALOG(R)File 348:(c) 2002 European Patent Office. All rts. reserv.

Office environment level electrostatic discharge protection
Elektrostatische Entladungsschutzvorrichtung fur Buroraume
Protection contre des decharges electrostatiques a un niveau d'environnement de bureau
PATENT (CC, No, Kind, Date): EP 590859 A2 940406 (Basic)
EP 590859 A3 951122
EP 590859 B1 011219

...52) in response to a voltage between the connector (32) and ground (52) in excess of a predetermined threshold. A zone (90) of a predetermined **electrical** resistance is operatively disposed between the bipolar transistor (66-70) and ground (52). The zone (90) may substantially encircle (Fig 4) the bonding pad (32) of the connector to evenly distribute **local** incidences of high voltage. The invention enables **integrated circuits** to pass ESD requirements of office products, which is 15kV by Human Body Model testing. (see image in **original** document)

9. A **printer** as in claim 8, wherein the protection device (60) comprises a **MOS** field effect device (60) with a bipolar transistor (66-70) parasitic thereto, the bipolar transistor (66-70) having a collector (66), an emitter (68), and...

39/TI,PN,PD,PY,K/7 (Item 7 from file: 348)

Monolithic **integrated circuit** chip for a **thermal ink jet printhead**
Monolithischer integrierter Schaltkreis-Chip fur Thermo-Farbstrahldruckkopf
Microplaquette de **circuit** integre monolithique pour tete d'impression thermique par jet d'encre
PATENT (CC, No, Kind, Date): EP 494076 A2 920708 (Basic)
EP 494076 A3 921021
EP 494076 B1 970917

A **thermal** jet ink **printing** system is provided with an improved **printhead** (11). The **printhead** (11) is formed by monolithic integration of **MOS** logic elements and drivers onto the same silicon **substrate** (41) containing the resistive elements using a more efficient manufacturing process. In a preferred embodiment, the logic switches, logic drivers and resistive elements are formed from a single layer of polysilicon with the resistive element formed on a thermally grown field oxide layer (125). The **integrated circuit** chips (110) are formed by a **MOS** fabrication technology which uses fewer processing steps than used in existing chips, and the resulting chips are thermally stable and can be operated at higher logic voltages. (see image in **original** document)

10. A method of fabricating a **thermal ink jet printing** module having a monolithic **integrated circuit** which contains logic (112, 114), driver (116) and resistor (118) elements on the surface of a common silicon wafer (146), comprising the steps of:
forming patterned polysilicon gate regions (128) on a gate oxide layer (126) disposed on the surface of the **substrate** (146), said gate regions (128) defining gate channels in the **substrate** thereunder located adjacent said channels;
(9) forming a **sacrificial** oxide layer over the **substrate** surfaces exposed in step (8);
(10) patterning the **substrate** with a second photoresist layer, wherein the unmasked portions bounded by said second photoresist layer define depletion logic regions of the underlying **substrate**;
(11) ion implanting the depletion logic regions of the **substrate** with a n-type depletion mode dopant;
(12) stripping said second photoresist layer, and etching the **substrate** to remove the **sacrificial** oxide layer and expose the silicon **substrate** therebelow;
(16) ion implanting said polysilicon layer (228) with n-type ions to reduce the sheet resistance of said polysilicon layer;
(17) after said patterning the...
...129) semiconductive polysilicon regions and the unmasked regions being subsequently etched way, whereby said gate polysilicon regions further define gate channels therebelow, within the silicon **substrate**, and whereby said polysilicon resistor regions are disposed on the upper surface of the field oxide layer (125); and

39/TI,PN,PD,PY,K/8 (Item 8 from file: 348)

Monolithic silicon **integrated circuit** chip for a **thermal ink jet printer**
Monolithisch integrierte Siliciumschaltkreis fur einen Thermotintenstrahldr ucker
Puce de **circuit** integre monolithique en silicium pour une imprimante thermique a jet d'encre
PATENT (CC, No, Kind, Date): EP 401440 A1 901212 (Basic)
EP 401440 B1 990915

A **thermal** jet ink **printing** system is provided with an improved **printhead**. The **printhead** is formed by monolithic integration of **MOS** transistors switches (78, 80, 82) onto the same silicon **substrate** (48) containing the resistive elements. In a preferred embodiment, the transistor switches and resistive elements are formed from a single layer of polysilicon (78, 79) with the resistive element formed on a thermally grown field oxide layer (72) having a thickness ranging from about one to four (mu)m. The **integrated circuit** chips are formed by **MOS** technology, are thermally stable and can be operated at higher voltages than known chips. ...

2. The monolithic silicon **integrated circuit** chip of claim 1, wherein a single layer of polysilicon is used for the gate (78) of the transistor switch and for the resistive element (79).
3. The monolithic silicon **integrated circuit** chip of claims 1 or 2, wherein the chip is formed from a p type silicon wafer.
4. A **thermal ink jet printhead** including the monolithic silicon **integrated circuit** chip of any one of claims 1 to 3.

39/TI,PN,PD,PY,K/9 (Item 9 from file: 348)

Integrated **thermal ink jet printhead** and method of manufacture.
Integrierter Warmetintenstrahl-Druckkopf und Herstellungsverfahren.
Tete integree d'imprimante a gicleur d'encre thermique et la methode de manufacture.
PATENT (CC, No, Kind, Date): EP 229673 A2 870722 (Basic)
EP 229673 A3 890726
EP 229673 B1 920708

This application discloses a **thermal ink jet printhead** and related **integrated** pulse driver **circuit** useful in **thermal ink jet printers**. This combined **printhead** and pulse drive **integrated circuit** includes a first level (5,6) of metallization comprising a refractory metal which is patterned to define the **lateral** dimension of the **printhead** resistor (4). A passivation layer or layers (7,8,9) are deposited atop this first level (5,6) of metalization and patterned to have an opening or openings therein for receiving a second level (10,11) of metalization. This second level (10,11) of metallization such as **aluminium** may then be used for electrically interconnecting the **printhead** resistors (4) to **MOSFET** drivers and the like which have been fabricated in the same silicon **substrate** (1) which provides suport for the **printhead** resistors (4). Thus, this "on-chip" driver construction enables these pulse driver transistor to be moved from **external** electronic **circuitry** to the **printhead substrate**.

a

plurality of heater resistors and to provide a **path** for drive current to predefined areas in said resistive heater layer (4), and forming a multilevel metal **integrated circuit** including a metal interconnect (10,**11**) between a **metal-oxide-semiconductor** (**MOS**) driver **circuit** and said refractory metal (5,6).

2. The process defined in claim, 1, characterized in that said refractory silicide (4) is selected from the group consisting of **tantalum silicide**, titanium silicide, tungsten silicide and **molybdenum silicide**, and said refractory metal (5,6) is selected from the group consisting of **tantalum**, **titanium**, tungsten and **molybdenum**.

3. An electronic device comprising a supporting **substrate** (1), a resistive heater, layer (4) of resistive **material** selected from **the group** consisting of polycrystalline silicon and a refractory silicide and disposed above said **substrate to define the**

. **The device defined in claim 3, characterized in that said refractory silicide (4) is selected from** the group consisting of **tantalum** silicide, titanium silicide, tungsten silicide and **molybdenum** silicide, and said refractory metal (5,**6**) is selected from the group consisting of **tantalum**, titanium, tungsten and **molybdenum**.

5. Electronic device according to claim 3 or 4, characterized in that said resistive layer (4) is protected on selected areas **of** both sides by **silicon nitride** (3,

39/TI,PN,PD,PY,K/10 (Item 10 from file: 349)

A THERMALLY ACTUATED INK JET
JET D'ENCRE A COMMANDE THERMIQUE
Patent and Priority Information (Country, Number, Date):
Patent: WO 9903681 A1 19990128
Publication Year: 1999

...as to maintain said 5 actuator substantially in a predetermined position. 328. A thermal actuator including a lever arm attached at one end to a **substrate**, said thermal actuator being operational as a result of conductive heating of a conductive trace, said conductive trace including a thinned cross-section substantially adjacent said attachment to said **substrate**. 329. An **ink jet** nozzle arrangement for the ejection from a nozzle chamber out of an ink ejection 0 nozzle, said arrangement comprising:
a nozzle charnber for the storage...
An **ink** **jet** nozzle arrangement as claimed in claim 340 wherein said arrangement is formed adjacent to neighbouring arrangements so as to form a pagewidth **print head**.
5 351. An **ink jet** nozzle arrangement comprising:
a nozzle chainber for storage of ink to be ejected from an ink ejection nozzle formed in one wall of the nozzle...
An **ink jet** nozzle arrangement as claimed in claim 354 wherein said silicon wafer is initially processed utilizing a **CMOS** processing system so as to form the electrical **circuitty** required to operate said **ink jet** nozzle arrangement on said silicon wafer. 5 364. A method of manufacturing a planar thermoelastie bend actuator **ink jet print head** wherein an array of nozzies are forined on a **substrate** utilising planar monolithic deposition, lithographic and etching processes. 365. A method as claimed in claim 364 wherein multiple **ink jet** heads are formed simultaneously on a single planar **substrate**. 366. A method as claimed in claim 365 wherein said **substrate** is a silicon wafer. 0 367. A method as claimed in claim 364 wherein said **print heads** are formed utilising standard vlsi/ulsi processing. 368. A method as claimed in claim 364 wherein integrated drive electronics are formed on the same **substrate**. 369. A method as claimed in claim 368 wherein said integrated drive electronics comprise a **CMOS** 5 process. 370. A method of manufacturing a pump action **ink jet print head** wherein an array of nozzles are formed on a **substrate** utilising planar monolithic deposition, lithographic and etching processes. 371. A method as claimed in claim 370 wherein multipie **ink jet** heads are formed simultaneously on a single planar **substrate**
...wherein said step (b) comprises a crystallographic etch of said wafer. 380. A method as claimed in claim 377 wherein said conductive layers comprise substantially gold

...said first and second expansion material layers comprise substantially

polytetrafluroethylene. 401. A method as claimed in claim 398 wherein said inert material layer comprises substantially silicon nitride

A method of manufacturing a buckle grill oscillating pressure ink jet print head wherein an array of nozzles are formed on a **substrate** utilising planar monolithic deposition, lithographie and etching processes. 5 407. A method as claimed in claim 406 wherein multiple **ink jet** heads are forined simultaneously on a single planar **substrate**

...**first and second expansion material layers 0 comprise substantially polytetrafluroethylene. 415. A method as claimed in claim 412 wherein said inert material layer comprises substantially silicon nitride**. 416. A method as claimed in claim 412 wherein said ink supply channel is forined by etching a channel from the back surface of said...

A method as claimed in claim 434 wherein said inert material layer comprises substantially **silicon nitride**

.**said arrangement so as to reduce cor-rosion effects. 442. A method as claimed in claim 434 wherein said wafer comprises a double side polished CMOS** wafer. 443. A method as claimed in claim 434 wherein said steps are also utilized to simultaneously separate said wafer into separate **printheads**. 444. A method of a thermal actuated **ink jet print head** wherein an array of nozzles are formed on a **substrate** utilising planar monolithic deposition, lithographic and etching processes. 0 445. A method as claimed in claim 444 wherein multiple **ink jet** heads are formed simultaneously on a single planar **substrate**

45/TI,PN,PY,PD,K/1 (Item 1 from file: 348)

Ink-jet element substrate, **ink-jet** printing head and **ink-jet** printing apparatus
Substrat fur ein Element eines Tintenstrahldruckkopfes, Tintenstrahldruckkopf und Tintenstrahldruckapparat
Substrat pour element a jet d'encre, tete d'impression a jet d'encre et appareil d'impression a jet d'encre
PATENT (CC, No, Kind, Date): EP 805029 A2 971105 (Basic)
EP 805029 A3 980624
EP 805029 B1 020320

CLAIMS 1. A substrate for an **ink-jet** element of an **ink-jet** printing head ejecting an ink through a plurality of ejection openings, characterized by comprising:
a plurality of heating elements provided for each of said plurality of ejection openings and generating a **thermal** energy for ejecting the ink;
2. A substrate for an **ink-jet** element as set forth in claim 1, characterized in that said data holding circuit and said selection circuit are integrally built-in said substrate for the **ink-jet** element.
elements.
15. A substrate for an **ink-jet** element as set forth in claim 1, characterized in that said heating element is a **electrothermnal** transducer.
25. An **ink-jet** printing head as set forth in claim 16, characterized in that said driving circuit includes a **N-MOS** transistor.
..CLAIMS B1
1. A substrate for an **ink jet print head** for ejecting ink through a plurality of ejection openings, the substrate comprising:
heating elements (201(1).. 201(n)) for generating **thermal** energy to cause ink **ejection**, the heating **elements** being arranged to provide a respective plurality of heating elements for each of said plurality of ejection openings;

45/TI,PN,PY,PD,K/2 (Item 1 from file: 349)

ALIGNING METHOD FOR MULTIPLE **INK JET** COLOUR **PRINTHEADS** WITH BUILT-IN OPTOELECTRONIC POSITION DETECTOR
PROCEDE D'ALIGNEMENT DE PLUSIEURS TETES D'IMPRIMANTE COULEUR A JET D'ENCRE, A L'AIDE D'UN CAPTEUR DE POSITION OPTOELECTRONIQUE INTEGRE

Patent and Priority Information (Country, Number, Date):
Patent: WO 200058101 A1 20001005 (WO 0058101)
Publication Year: 2000

English Abstract
The single heads (40) mounted on a single print carriage of an **ink jet** printer comprise a column (50) of phototransistors (5l-i), built directly into the chip of each head in the same process steps as used for...

23 **Ink jet** dot-matrix **printhead** comprising:
a semiconductor substrate;
a first plurality of **ejection elements** integrated on said substrate, for the generation of droplets of ink through a corresponding plurality of nozzles, arranged at a constant pitch in at least one row according to a first vertical direction;
a second plurality of electronic components integrated on said substrate by means of a **C-MOS** technology for selecting and driving said first plurality of **ejection elements**,
characterized in that it further comprises a column (50) made up of a plurality of phototransistors (5 I-i) integrated on said substrate by means of said **C-MOS** technol

30 **Ink jet** dot-matrix **printhead** comprising:
1 5 - a semiconductor substrate;
a first plurality of **ejection elements** integrated on said substrate, for the generation of droplets of ink through a corresponding plurality of nozzles, arranged at a constant pitch 'in at least one row according to a first vertical direction;
- a second plurality of electronic components integrated on said substrate by means of a **C-MOS** technology for selecting and driving said first plurality of **ejection elements**;

53/TI,PN,PD,PY,K/1 (Item 1 from file: 348)

Integrated thin-film drive head for **thermal ink-jet** printer
Kopf mit integriertem Dunnfilmtrieb fur warmegetriebene Tintenstrahldrucker
Tete de commande integree a couche mince pour imprimante thermique a jet d'encre
PATENT (CC, No, Kind, Date): EP 778139 A1 970611 (Basic)
EP 778139 B1 000202

..ABSTRACT A1

A thin-film **ink-jet** drive head provides a MOSTFT (**metal oxide semiconductor** thin-film **transistor**) **transistor** (32), a resistor (26) and the interconnect between the two **electrical** components (46d), all comprised of the same, multi-**functional** thin-film layer (46). Differing portions of the multi-**functional** thin-film layer function as, (1) heating resistors to propel ink droplets from the **printhead** (20), (2) ink MOSTFT **transistors** to selectively drive (fire) the resistors, and (3) direct conductive pathways between the drive **transistors** and the resistors.

CLAIMS 1. A drive head for a **thermal ink-jet printhead** device (20) comprising:
a switching device (32);
a heat transducer (26), spaced from the switching device; and
a multi-**functional** layer (46) deposited on a substrate (40, 42) and having a first portion that functions as an active portion (46b) of the switching device and having a second portion (46e) that functions as a portion of the heat transducer. and wherein
the multi-**functional** layer also includes a conductive third portion (46d) that is integrally formed with the first and second portions (46b, 46e) and is continuous therewith to thus interconnect the first and second portions (46b, 46e) so that the third portion (46d) carries **electrical** signals between the switching device and the heat transducer.

2. The drive head of claim 1 including an ink chamber (16) assembly attached thereto, the ink chamber assembly including an ink barrier (72) and a plate member (76) positioned above the ink barrier, the plate member having an opening for **ejecting** an ink droplet therethrough.

7. A method for fabricating a drive head for a **thermal ink-jet printhead** device (20) comprising the steps of:
providing a substrate (40, 42);

53/TI,PN,PD,PY,K/2 (Item 2 from file: 348)

Ink-jet print head thermal working condition stabilization method
Stabilisierungsverfahren des thermischen Betriebszustandes eines Tintenstrahldruckkopfes
Methode de stabilisation de l'etat thermique de fonctionnement d'une tete d'impression a jet d'encre

PATENT (CC, No, Kind, Date): EP 752313 A2 970108 (Basic)
EP 752313 A3 970723
EP 752313 B1 010404

An **ink jet printhead** comprising a plurality of **ejection** resistors and at least one **additional** resistor (11), integrated on the same semiconductor substrate; the **additional** resistor is constituted by a **material** with a positive coefficient of variation of resistance with temperature of between 0.3 and 1.0%/(degree)C and is used both for heating of the substrate and for measuring its temperature(Ts))). Various circuits based on using the **additional** resistor are defined for implementing a method for stabilizing temperature of the substrate; also defined are a method for obtaining a stabilization temperature that remains constant with variation of the characteristics of the head and a method for setting the energetic operating point (El))) of the **ejection** resistors.

CLAIMS 1. An **ink jet printhead** comprising at least one **ejection** resistor integrated on a semiconductor substrate for **ejecting** droplets of ink, said substrate having a temperature (Ts))), characterised in that said **printhead** further comprises at least one second resistor (11) having a determined resistance value (RA))) integrated on said substrate for heating said substrate and for measuring said temperature (Ts))) of said substrate.

2. An **ink jet printhead** according to claim 1,

3. An **ink jet printhead** according to claim 1, characterised in that said at least one second resistor (11) is constituted by a **material** selected in a group consisting of **copper**, **aluminium**, and **aluminium/copper** alloys.

6. A method according to claim 5, characterised in that said first energy supplying means comprise at least one **MOS transistor** (18) integrated on said semiconductor substrate.
amount is between 2% and 50% of said first energy value (Eg))).

15. A method for automatically setting the energetic operating point of **ejection** resistors of an **ink jet printhead**, said **printhead** including:

53/TI,PN,PD,PY,K/3 (Item 3 from file: 348)

Ink-jet print head with integrated driving components
Tintenstrahldruckkopf mit integrierten Betatigungskomponenten
Tete d'impression a jet d'encre avec composants de commande integres
PATENT (CC, No, Kind, Date): EP 749834 A2 961227 (Basic)
EP 749834 A3 970723
EP 749834 B1 010404

.ABSTRACT A2
In an **ink jet printhead** (100) comprising **ejection** resistors (Ri) and **MOS transistors** (TRi) for supplying the resistors the energy for **ejecting** droplets of ink, integrated on the same semiconductor substrate, a given range of values is defined for the ratio of the channel resistance (Rc) during conduction of the **MOS transistor** to the resistance (R) of the **ejection** resistor so that the energetic operating point (El) of the **ejection** resistor is automatically compensated for variations in temperature (Ts) of the substrate, thereby assuring quality of printing and preventing **ejection** resistor conditions of operation liable to damage the resistor itself. (see image in **original** document)

1. An **ink-jet print head** (100) comprising at least one resistor (Ri) for **ejecting** droplets of ink, and at least one **MOS transistor** (Tri) for supplying energy to said at least one resistor, said at least one resistor and said at least one **MOS transistor** being both integrated on a common semiconductor substrate, characterised in that it further comprises compensation means for automatically compensating the energetic operating point (El) of said at least one resistor with respect to changes in temperature (Ts) of said common substrate.
2. An **ink-jet print head** according to claim 1,
4. An **ink-jet print head** comprising at least one resistor (Ri) for **ejecting** droplets of ink having a resistance value R, and at least one **MOS transistor** (TRi) for supplying energy to said resistor having a channel resistance during conduction of value Rc, characterised in that the ratio Rc/R has a determined value of between 0.10 and 0.25.

CLAIMS 1. An **ink-jet print head** (100) comprising at least one resistor (Ri) for **ejecting** droplets of ink, and at least one **MOS transistor** (Tri) for supplying a working energy (El) to said at least one resistor (Ri), said at least one **MOS transistor** (Tri) having a channel resistance (Rc), said at least one resistor and said at least one **MOS transistor** being both integrated on a common semiconductor substrate, said **ink-jet print head** (100

53/TI,PN,PD,PY,K/4 (Item 4 from file: 348)

Office environment level electrostatic discharge protection
Elektrostatische Entladungsschutzvorrichtung fur Buroraume
Protection contre des decharges electrostatiques a un niveau d'environnement de bureau
PATENT (CC, No, Kind, Date): EP 590859 A2 940406 (Basic)
EP 590859 A3 951122
EP 590859 B1 011219

...ABSTRACT A2
An electrostatic discharge protection (ESD) device for a connector associated with an integrated circuit chip, particularly one associated with a **thermal ink-jet printhead**. A **MOS** field effect device (60) extends along at least one edge of the connector (32) on the chip. A bipolar **transistor** (66-70), parasitic to the field effect device (60), conducts current from the connector (32) to ground (52) in response to a voltage between the connector (32) and ground (52) in excess of a predetermined threshold. A zone (90) of a predetermined **electrical** resistance is operatively disposed between the bipolar **transistor** (66-70) and ground (52). The zone (90) may substantially encircle (Fig 4) the bonding pad (32) of the connector to evenly distribute **local** incidences of high voltage. The invention enables integrated circuits to pass ESD requirements of office products, which is 15kV by Human Body Model testing. (see image in **original** document)

electrostatic discharges.

9. A printer as in claim 8, wherein the protection device (60) comprises a **MOS** field effect device (60) with a bipolar **transistor** (66-70) parasitic thereto, the bipolar **transistor** (66-70) having a collector (66), an emitter (68), and a base (70), and adapted to conduct current from the connector (30,32) to ground...

..32,30) and ground (52) in excess of a predetermined threshold; characterized by

a negative feedback resistance formed by a semiconductor region (90) of a **substantial electrical** resistance operatively disposed, at the emitter side, between the base (68) of the bipolar **transistor** (66-70) and ground (52), the semiconductor region (90) extending along at least one edge of the connector along the surface of the apparatus, whereby the resistance acts as a negative feedback loop controlling the current flow from the emitter to the collector of the bipolar **transistor** along the edge of the connector.

2. A electrostatic discharge protection device as in claim 1, wherein the connector comprises a substrate (30) and a...

...on the surface of the substrate (30).

3. A electrostatic discharge protection device as in claim 2, wherein the field oxide device (60) and/or **transistor** (66-70) is operatively disposed continuously along an edge of the bonding pad (32); and/or wherein the field oxide device (60) and/or **transistor** (66-70) substantially encircles the bonding pad

(32).

4. A electrostatic discharge protection device as in claim 2 or 3, wherein the collector (66) of the **transistor** is connected to the bonding pad (32) with the emitter (68) being connected to ground (52); and preferably wherein the base (70) of the **transistor** comprises a channel-stop implant in the substrate (30).
5. A electrostatic discharge protection device as in any of claims 2 to 4, wherein the...

53/TI,PN,PD,PY,K/5 (Item 5 from file: 348)

Ink jet recording system
Tintenstrahlaufzeichnungssystem
Systeme d'enregistrement a jet d'encre
PATENT (CC, No, Kind, Date): EP 440459 A1 910807 (Basic)
EP 440459 B1 970806

Ink jet recording system

...ABSTRACT A1
A recording head (IJC) comprises **electrothermal** transducers (940) for jetting ink and **functional** devices (1-19, 50) for driving these **electrothermal** transducers (940), both of which are arranged on a single substrate plate (1). The **functional** devices comprise a pair of major electrode regions (4,5) such as drain and source arranged on the substrate plate (1), a region (19) comprising...
plate.

3. A substrate as claimed in claim 1, characterized in that said plurality of energy generating members are a plurality of **thermal** transducers for generating **thermal** energies in correspondency with driving signals from said plurality of **functional** devices, said **thermal** energies cause film boiling in ink and thereby **eject** ink from said ink **ejection** outlet.

4. A substrate as claimed in claim 2, characterized in that said plurality of energy generating members are a plurality of **thermal** transducers for generating **thermal** energies in correspondency with driving signals from said plurality of **functional** devices, said **thermal** energies cause film boiling in ink and thereby **eject** ink from said ink **ejection** outlet.

30. A substrate for a printer head comprising a plurality of **electrothermal** transducers and a plurality of control or **functional** components, comprising **MOS transistors** characterised in that the **transistors** are arranged as an array each **transistor** having a channel region arranged to improve the **transistor** breakdown voltage.

53/TI,PN,PD,PY,K/6 (Item 6 from file: 349)

INKJET PRINTHEAD WITH TWO-DIMENSIONAL NOZZLE ARRANGEMENT AND FABRICATING METHOD THEREFOR
TETE D'IMPRESSION A JET D'ENCRE COMPORTANT UN DISPOSITIF DE BUSE BIDIMENSIONNELLE ET PROCEDE DE FABRICATION ASSOCIE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200183220 A1 20011108 (WO 0183220)
Publication Year: 2001

An **inkjet printhead** for high-resolution and high-speed printing and its fabricating method. The improved printing capability is accomplished by two-dimensional nozzle and ink feed hole arrangement in a **printhead** substrate. Conventional **printheads** where nozzles are arranged around an ink feed hole in a row usually have a problem of low level integration. However, according to the present invention, a number of nozzles can be integrated in the substrate, allowing the **printhead** to be operated at high speed and high resolution.

Claim
1 An **inkjet printhead** comprising:
a substrate having at least four ink-supply path orifices arranged in a two-dimensional array;
at least one nozzle connected to each of the ink-supply path orifices;
driving means for driving the nozzles; and
electrical devices for decoding electric signals provided from outside the **inkjet printhead** and transmitting the decoded electric signals to the driving means in order to selectively drive the nozzles.
The et **printhead** as claimed in claim 1, wherein the two-dimensional array of the ink-supply path orifices is a n x n array or a I x n array, wherein n is a natural number (Yreater than 2.
ZD

6 The **inkjet printhead** as claimed in claim 1, wherein the electrical device is a switchino device sucli as a diode or a metal-oxide-silicon (**MOS**) **transistor** and is
8 The **inkjet printhead** as claimed in claim 1, wherein the two-dimensional array of ink-supply path orifices and nozzles comprises rows forming a certain angle with respect to a print-movement direction of the **inkjet printhead**.

9 The **inkjet printhead** as claimed in claim 1, wherein the nozzles are arranged in array blocks, and different color ink is supplied to each array block to enable printing of a plurality of colors. I 0 10.
A method of fabricating an **inkjet printhead**, the method comprising the
steps of:
sequentially forming a silicon oxide layer and a **silicon nitride** layer on a
'I'con substrate doped with a first conductive-type impurity;
si I
etching the silicon oxide layer and the **silicon nitride** layer except in a 1 5 switching device area and a main ink-supply path area to

08/13/2002 09/813,087

53/TI,PN,PD,PY,K/7 (Item 7 from file: 349)
DIALOG(R)File 349:(c) 2002 WIPO/Univentio. All rts. reserv.

DRIVE CIRCUIT FOR A THERMAL **INK JET PRINTHEAD**
CIRCUIT D'ATTAQUE POUR UNE TETE D'IMPRESSION THERMIQUE A JET D'ENCRE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200061372 A1 20001019 (WO 0061372)
Publication Year: 2000

English Abstract
This invention relates to an integrated circuit for the driving of **ink jet printheads**. The circuit (10) comprises a thermal resistor (11) for generating a bubble of steam and **ejecting** a droplet of ink, a logic drive circuit (14, 15) and a power **transistor** (12) connected to the thermal resistor (11) and controlled directly by the logic circuit (14, 15). The **transistor** (12) is made from the same technology as the logic circuit (14, 15) and is driven with a gate voltage V<sb>G of between...

...and 5.5 Volts. The circuit (10) does not require the insertion of voltage boost devices between the logic circuit (14, 15) and the power **transistor** (12) while guaranteeing a low total resistance R<sb>ON of the **transistor**, in practice in the region of 3.5(divided by)4.5

3 Drive circuit according to claim 1. characterised in that said power **transistor** (12) is **NMOS** or NDDD-**NMOS** type.

7 Circuit according to claim 1, 2 or 3 characterised in that said power **transistor** (12) has a threshold voltage VTH of between 0.6 and 1.0 V (volt).

53/TI,PN,PD,PY,K/8 (Item 8 from file: 349)

IMPROVEMENTS RELATING TO **INKJET** PRINTERS
AMELIORATION D'IMPRIMANTES A JET D'ENCRE
Patent and Priority Information (Country, Number, Date):
Patent: WO 200023279 A1 20000427 (WO 0023279)
Publication Year: 2000

English Abstract
An **inkjet printhead** having a series of nozzles for the **ejection** of ink wherein each said nozzle has a rim formed by the deposition of a rim material layer (42) over a sacrificial layer (41) and ...

laim
I - An **inkJet printhead** having a series of nozzles for the **ejection** of ink wherein each said nozzle has a rim formed by the deposition of a rim material layer over a sacrificial layer and a subsequent planar removal of at least said rim material layer so as to form said nozzle rim.

17 A method as claimed in claim 16 wherein said electrical drive circuitry comprises a Complementary **Metal Oxide Semiconductor** (**CMOS**) process.

18 A method as claimed in claim 16 wherein said sacrificial material layer comprises a **CMOS** metal layer.

21 An inkj et **printhead** constructed by MEMS processing techniques with a plurality of ink **ejection** nozzles each having a nozzle chamber, an external thermal bend actuator having a proximal end anchored to a substrate and a distal end connected to an ink **ejection** paddle within said chamber;

46 A method of operation of a fluid **ejection printhead** within a predetermined thermal range so as to print an image, said **printhead** including a series of then-nal actuators operated to **eject** fluid from said **printhead,** said method comprising the steps of-. (a) sensing the **printhead** temperature of said **printhead** to determine if said **printhead** temperature is below a predetermined threshold, (b) if said **printhead** temperature is below said predetermined threshold, performing a preheating step of heating said **printhead** so that it is above said predetermined threshold, (c) controlling said preheating step such that said thermal actuators are heated to an extent insufficient to cause the **ejection** of fluid from said **printhead**

```
 (FILE 'HOME' ENTERED AT 15:32:20 ON 13 AUG 2002)

     FILE 'REGISTRY' ENTERED AT 15:32:40 ON 13 AUG 2002
                E SILICON DIOXIDE
                E (SILICON DIOXIDE)/CN
                E SILICON DIOXIDE/CN
                E SILICON NITRIDE/CN
                E SILICON DIOXIDE/CN
L1              1 S E3
                E SILICON NITRIDE/CN
L2              1 S E3
                E SILICON CARBIDE/CN
L3              1 S E3
                E TANTALUM/CN
L4              1 S E3
                E ALUMINIUM/CN
L5              1 S E3
                E ALUMINUM/CN
L6              1 S E3
                E COPPER/CN
                E GOLD/CN
                E COPPER/CN
L7              1 S E3
                E GOLD/CN
L8              1 S E3
                E TUNGSTEN/CN
L9              1 S E3
                E MOLYBDENUM/CN
L10             1 S E3
L11             9 S L1-L10

     FILE 'CAPLUS' ENTERED AT 15:38:17 ON 13 AUG 2002
L12        311129 S (SILICON()DIOXIDE) OR SI02 OR QUARTZ OR (SILICON()NITRIDE) OR
L13       2660071 S TANTALUM OR TA OR ALUMINIUM  OR ALUMINUM OR AL OR COPPER OR C
L14       3040713 S L13 OR L12 OR L11
L15         40726 S (MOS OR METAL()OXIDE(1W)SEMICONDUCT OR NMOS OR N()MOS OR PMOS
L16         18192 S MOSFET OR MOS()FET OR METAL()OXIDE(1W)SEMICONDUCT######
L17         25843 S (FIELD()EFFECT()TRANSIST########) OR FET
L18            11 S L15:L17
L19         50886 S INTEGRAT########(3N)(CIRCUIT####### OR LOOP)
L20           872 S (PRINTHEAD OR PRINT()HEAD)
L21          2294 S (FLUID OR LIQUID)()JET OR FLUIDJET
L22         14921 S INKJET OR INK()JET OR INK()JETT### OR INKJETT
L23        802313 S SUBSTRATE
L24        271429 S (INSULAT#### OR OXIDE OR DIELECTRIC####)(3N)(LAYER#### OR FIL
L25         37655 S L14 AND L15
L26             0 S L25 AND L18
L27          5083 S L25 AND L19
L28             1 S L27 AND L20
L29          5082 S L27 NOT L28
L30             0 S L29 AND L21
L31             1 S L29 AND L22
L32          5081 S L29 NOT L31
L33          1711 S L32 AND L23
```

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L34        1478 S L32 AND L24
L35           0 S L34 AND (CARRIAGE OR CARTRIDGE)
L36           0 S L34 AND (FLUID OR LIQUID)(3N)(RESERVOIR OR CHANNEL#####)
L37           3 S L34 AND (RECORD#######(3N)DEVICE)
L38        1475 S L34 NOT L37
L39           0 S L38 AND ((PRESSUR? OR COMPRESS?)(3N)(REGULAT? OR CONTROL? OR
L40           0 S L38 AND (AIR(3N)(PRESSUR? OR COMPRESS?))
L41           0 S L38 AND (EJECT?(3N)ELEMENT)
L42          56 S L38 AND (PHOSPHOSILICATE OR PHOSPHO()SILICATE)
L43           1 S L42 AND (THERMAL?(3N)OXIDE)
L44          55 S L42 NOT L43
L45           7 S L44 AND (GATE(3N)OXIDE)
L46           7 DUP REM L45 (0 DUPLICATES REMOVED)
L47           7 S L46
L48          48 S L44 NOT L46
L49          22 S L48 AND TRANSISTOR
L50           0 S L49 AND L18
L51          22 DUP REM L49 (0 DUPLICATES REMOVED)
```

L28 ANSWER 1 OF 1 CAPLUS COPYRIGHT 2002 ACS
AN 1992:162615 CAPLUS
DN 116:162615
TI Method of fabricating a monolithic **integrated circuit** chip for a thermal ink-jet **print head**
IN Hawkins, William G.; Burke, Cathie J.
PA Xerox Corp., USA
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5075250	A	19911224	US 1991-636826	19910102

AB A thermal printing app. is provided with an improved **print head**. The **print head** is formed by monolithic integration of **MOS** logic elements and drivers onto the same Si substrate contg. the resistivie elements using a more efficient manufg. process. In a preferred embodiment, the logic switches, logic drivers, and resistive elements are formed from a single layer of poly/Si with the resistive element formed on a thermally grown field oxide layer. The **integrated circuit** chips are formed by a **MOS** fabrication technol. which uses fewer processing steps than used in existing chips, and the resulting chips are thermally stable and can be operated at higher logic voltages.

L31 ANSWER 1 OF 1 CAPLUS COPYRIGHT 2002 ACS
AN 2002:533995 CAPLUS
DN 137:101447
TI Method of forming **ink-jet** printing head using part of active circuitry layers to form sacrificial structures
IN Silverbrook, Kia
PA Silverbrook Research Pty. Ltd., Australia
SO U.S., 86 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6420196	B1	20020716	US 1999-425194	19991019
PRAI	AU 1998-6535	A	19981016		

AB An **ink-jet** printing head is formed on a substrate incorporating drive circuitry for the nozzles of the printing head formed by a **CMOS** process. One or more of the layers formed by the **CMOS** process are utilized as a sacrificial material layer in forming the actuators or paddles of the ink ejection nozzles formed by MEMS process. The object of the present invention is to provide for the effective utilization of each masking layer in the construction of a micro-electro mech. system such as an **ink-jet** printing head.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L37 ANSWER 1 OF 3 CAPLUS COPYRIGHT 2002 ACS
AN 2000:367145 CAPLUS
DN 132:355637
TI Semiconductor devices having a thin film field-effect transistor and corresponding manufacturing methods
IN Yamazaki, Shunpei
PA Semiconductor Energy Laboratory Co., Ltd., Japan
SO Eur. Pat. Appl., 60 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1005094	A2	20000531	EP 1999-123427	19991124
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2000223716	A2	20000811	JP 1999-334453	19991125
PRAI	JP 1998-333623	A	19981125		

AB The gate electrode of a non-amorphous TFT consists of a 1st gate layer (113,116) disposed on a gate **insulating film** (103) and made of a material selected from Si, **Ta**, Ti, W or **Mo** and compds. thereof, a 2nd gate layer (114,117) disposed on said 1st gate layer at a distance from the edge of said 1st gate layer and made of a low resistivity material such as **Cu** or **Al** and a 3rd gate layer (115,118) disposed on said 1st and 2nd gate layers and made of a material selected from Si, **Ta**, Ti, W or **Mo** and compds. thereof, thereby to enhance the thermal resistance of the gate electrode. Besides, such an n-channel TFT may be provided with a low-concn. impurity region (106a,106b) which adjoins a channel region (104), and which includes a 1st subregion (106a) overlapped by the gate electrode and a 2nd subregion (106b) not overlapped by the gate electrode, thereby to mitigate a high elec. field near the drain (108) of the TFT and to simultaneously prevent the OFF current of the TFT from increasing.

L43 ANSWER 1 OF 1 CAPLUS COPYRIGHT 2002 ACS
AN 1999:671071 CAPLUS
DN 131:280279
TI Nitride-sealed oxide-buffered local oxidation of silicon for forming isolation region in **integrated circuit**
IN Huang, Hsiu-wen; Hong, Gary
PA United Semiconductor Circuit Corp., Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5970364	A	19991019	US 1998-48697	19980326

AB The method includes forming a pad layer on a semiconductor substrate, and forming an oxidn. masking layer on the pad layer, wherein the pad layer relieves stress from the oxidn. masking layer. Next, portions of the oxidn. masking layer and the pad layer are patterned and etched. A first **oxide layer** is **thermally** grown on the substrate, and a second **oxide spacer** is formed on a sidewall of the pad layer and the oxidn. masking layer. After forming a nitride spacer on a surface of the second **oxide spacer**, the substrate is thermally oxidized to form the isolation region in the substrate.
RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L46 ANSWER 1 OF 7 CAPLUS COPYRIGHT 2002 ACS
AN 2002:585710 CAPLUS
TI Fabrication of self-aligned T-gate field-effect transistor with **gate oxide** sidewall protection
IN Lin, Hung-Jr; Wang, Meng-Fan; Lin, Chuan-Ding; Huang, Diau-Yuan
PA Shr, Min, Taiwan
SO Taiwan, 22 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI TW 388923	B	20000501	TW 1998-87118215	19981102

AB The method comprises forming a protective layer on the sidewall of a **gate oxide layer** to prevent that from being damaged by corrosion during the subsequent formation process of the T-gate, thereby avoiding lowering of performance of the **MOS** transistor. The present invention is carried out by a self-aligned process which uses planarization and forming a conductive stack layer on the polysilicon gate to obtain a T-gate conductive region, in order to reduce the parasitic resistance between the gate and the source/drain of the transistor. Furthermore, an air gap exists between the lower part of the stack conductive layer of the T-gate structure and an extension of the source/drain region, so that the parasitic capacitance between the gate and the source/drain can be reduced. Therefore, the present invention can be used for fabrication of high-speed and high-frequency **integrated circuits**.

L46 ANSWER 2 OF 7 CAPLUS COPYRIGHT 2002 ACS
AN 1999:582723 CAPLUS
DN 131:192929
TI Process for forming self-aligned metal silicide contacts for a **MOS** structure using a single silicide-forming step
IN Liu, Yauh-Ching; Giust, Gary K.; Castagnetti, Ruggero; Ramesh, Subramanian
PA LSI Logic Corporation, USA
SO U.S., 15 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5953614	A	19990914	US 1997-947742	19971009

AB A process is described for forming self-aligned contacts to an **MOS** device on an **integrated circuit** structure characterized by the simultaneous formation of the metal silicide gate portion and the metal silicide source/drain portions. The process comprises forming a **gate oxide layer** on a Si substrate, forming a polysilicon gate electrode **layer** over the **gate oxide layer**, and forming a **layer** of a 1st **insulation** material over the polysilicon gate electrode layer. Metal silicide is simultaneously formed on the exposed surface of the polysilicon gate electrode and over the exposed portions of the Si substrate. Source/drain regions are formed in the Si substrate, either before or after formation of the metal silicide over the exposed portions of the Si substrate, whereby the metal silicide portions on the substrate above the source/drain regions are in elec. communication with the source/drain regions.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L46 ANSWER 3 OF 7 CAPLUS COPYRIGHT 2002 ACS
AN 1997:809703 CAPLUS
DN 128:69652
TI Process for manufacturing a CMOSFET **integrated circuit**
IN Chen, Ming-Liang; Chu, Chih-Hsun
PA Mosel Vitelic Inc., Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5696016	A	19971209	US 1996-746765	19961115

AB The invention relates to a new process for fabricating **integrated circuits**, and more particularly, to a **CMOS** IC process of low cost, shallow junction, and no crystal defects. After the **gate oxide** and **gate** electrodes have been formed on the N-well and the P-well, an N- lightly doped drain (N- LDD) is made, then the sidewall of the N-channel polysilicon gate and the P-channel polysilicon gate are covered with **dielec. spacer**. A layer of **phosphosilicate** glass (PSG) is thereafter deposited and patterned on the N-well and the pickup area of the P-well by lithog. and etching. Ion implantation is used to build the P+ source/drain (S/D) electrode, after which the sidewall spacer of the P-channel polysilicon gate is removed and a blanket implantation of P forms the P- LDD on the area of the N-well. The P-well is doped with N-type dopant with its source from PSG by high-temp. diffusion and forms the N+ S/D electrode.

L46 ANSWER 4 OF 7 CAPLUS COPYRIGHT 2002 ACS
AN 1994:690892 CAPLUS
DN 121:290892
TI Multilayer polysilicon gate self-align process for VLSI **CMOS** device
IN Huang, Heng-Sheng; Chen, Kun-Luh; Hong, Gary
PA United Microelectronics Corp., Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5350698	A	19940927	US 1993-55567	19930503

AB A new method of forming a self-aligning polysilicon gate is described. A **gate** silicon **oxide** is formed over a silicon substrate. A polysilicon layer is formed over the **gate oxide**. A native silicon **oxide layer** is formed over the polysilicon layer. A 2nd polysilicon layer is formed over the native silicon **oxide layer**. Addnl. alternating layers of polysilicon and native silicon oxide are formed as desired. The wafer is annealed at .apprx.800-1000.degree.. This causes, it is believed, the silicon oxide gas from the multiple native silicon **oxide layers** to be exhausted, resulting in the removal of all silicon **oxide layers**. A polycide layer is formed overlying the multiple polysilicon layers, if desired. Conventional lithog. and etching techniques are used to form a gate. Ions are implanted into the substrate to form source/drain regions, using the multilayer gate as a mask. Rapid thermal annealing activates the impurities. A **dielec.** **layer** is deposited followed by conventional metalization techniques to complete construction of the **integrated** **circuit**.

L46 ANSWER 5 OF 7 CAPLUS COPYRIGHT 2002 ACS
AN 1991:620940 CAPLUS
DN 115:220940
TI Manufacture of **integrated circuits** containing bipolar and complementary-**MOS** transistors
IN Kato, Takao
PA Oki Electric Industry Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 03106066	A2	19910502	JP 1989-242308	19890920

AB The process includes: (a) forming a p-type diffusion layer (base) on the bipolar-transistor-planned region of a Si substrate; (b) forming SiO2 on the diffusion **layer**, and a **gate oxide film** on the complementary-**MOS**-transistor-planned region of the substrate; (c) removing a part of the SiO2 film to create an emitter-forming area; (d) forming a poly-Si film covering the SiO2 **film** and the **gate oxide film**; (e) forming, from the poly-Si, gate electrodes for the complementary-**MOS** transistor, and an electrode for the bipolar transistor; (f) forming a **phosphosilicate** glass film covering the electrodes; and (g) forming sidewalls for the electrodes by etching the glass film.

L46 ANSWER 6 OF 7 CAPLUS COPYRIGHT 2002 ACS
AN 1987:416321 CAPLUS
DN 107:16321
TI Semiconductor device
IN Takabayashi, Seiichiro; Sakata, Masanori; Yadoiwa, Yoshiaki
PA NEC Corp., Japan
SO Jpn. Tokkyo Koho, 3 pp.
CODEN: JAXXAD
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 62014941	B4	19870404	JP 1979-78485	19790621
	JP 56002638	A2	19810112		

AB A method for fabricating a moisture-resistant semiconductor device (e.g., Si-gate **MOS** large-scale **integrated circuit**) involves the following steps: (1) forming source and drain regions in a semiconductor substrate having field and **gate oxide films** and **gate** electrodes; (2) covering the field **oxide film**, **gate** electrodes, and source and drain regions with a high-concn. **phosphosilicate**-glass layer and then with an **oxide film** (0.2-1.5 .mu.m) contg. P2O5 1-7 mol%; (3) heat treating to make the **oxide film** more dense; (4) forming an **Al** interconnection connected to the source and drain regions; and (5) covering the overall surfaces with a vapor-deposited film.

L46 ANSWER 7 OF 7 CAPLUS COPYRIGHT 2002 ACS
AN 1979:431691 CAPLUS
DN 91:31691
TI Silicon gate **MOS integrated circuit**
IN Klein, Thomas
PA National Semiconductor Corp., USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 4151631	A	19790501	US 1977-798215	19770518
PRAI US 1976-725230		19760922		

AB **Integrated** Si-gate **MOS circuits** are manufd. without a sep. gate pad area. Polycryst. Si contacts are provided for the source and drain regions of polycryst. Si-gate transistors, so that subsequent metalization need only contact polycryst. Si. A thin layer of Si3N4 is deposited immediately after deposition of the polycryst. Si in the normal Si gate fabrication process. A polycryst. Si gate and interconnect pattern is etched in the Si3N4 and polycryst. Si layers. The exposed **gate oxide** is removed to provide automatic gate alignment and P is predeposited in the exposed Si substrate areas. A protective Si **oxide layer** is grown, with simultaneous P diffusion. No **oxide** grows on the **gate** and interconnect pattern because they are protected with Si3N4. The Si3N4 can be removed and contact made to polycryst. Si. The wafer is overcoated after nitride removal with a layer of **phosphosilicate** glass which is heated to provide a smooth surface and to getter impurities from the wafer. The polycryst. Si gates and contacts are simultaneously doped with P for cond. Contact holes are etched through the glass and interconnect pattern and **Al** metalization is applied and etched. Contacts to the polycryst. Si do not have to be precisely aligned. If there is contact offset, the grown oxide prevents shorting. The metal contacts touch only polycryst. Si, and not substrate or single-crystal Si.

L51 ANSWER 1 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 2002:237337 CAPLUS
DN 136:271655
TI Hydrogenated **silicon carbide** as liner for self-aligning contact vias in semiconductor **integrated circuit** fabrication
IN Dabbaugh, Gary; Gibson, Gerald W., Jr.; Giniecki, Troy A.; Steiner, Kurt G.
PA Agere Systems Guardian Corp., USA
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6362094	B1	20020326	US 2000-640329	20000816

AB The present invention provides a method of fabricating a self-aligning contact opening comprising: (a) forming a **dielec. layer** over a semiconductor substrate and gate electrodes located on the semiconductor substrate, (b) forming a carbide liner over the **dielec. layer**, and (c) etching at least a portion the carbide liner to form a self-aligning contact opening between the gate electrodes.
RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 2 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 2002:27859 CAPLUS
DN 136:93581
TI Production of semiconductor device comprising light-shielding metal layer for reflective liquid crystal projector showing improved light-shielding property
IN Saito, Toshio; Sakai, Hirotake; Matsumoto, Katsumi
PA Hitachi Ltd., Japan; Hitachi Device Engineering K. K.
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2002009074	A2	20020111	JP 2000-182762	20000619

AB In the prodn., first metal **film** pattern, an **insulating film**, and second metal film are successively formed on a substrate, and then the second metal film surface is polished to give a structure wherein the second metal film is buried in intervals of the first metal via the **insulating film**, so that light leakage via the **insulating film** is suppressed by thinning the **insulating film**. Prodn. of a **MOS integrated circuit** as a liq. crystal light valve for a reflective liq. crystal projector is also claimed. The liq. crystal projector shows improved light-shielding performance and brightness.

L51 ANSWER 3 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 2001:355102 CAPLUS
DN 134:347189
TI System and method for bonding over active **integrated circuits**
IN Saran, Mukul
PA Texas Instruments Incorporated, USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6232662	B1	20010515	US 1999-347212	19990702
PRAI US 1998-92961P	P	19980714		

AB An architecture and method of fabrication for an **integrated circuit** having a reinforced bond pad comprising .gtoreq.1 portion of the **integrated circuit** disposed under the bond pad; and this .gtoreq.1 circuit portion comprises .gtoreq.1 **dielec. layer** and a patterned elec. conductive reinforcing structure disposed in this .gtoreq.1 **dielec. layer.**
RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 4 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 2001:352321 CAPLUS
DN 134:347176
TI Trench photosensor for a **CMOS** imager
IN Rhodes, Howard E.
PA Micron Technology, Inc., USA
SO U.S., 19 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6232626	B1	20010515	US 1999-241080	19990201
	US 2001032979	A1	20011025	US 2001-782060	20010214
PRAI	US 1999-241080	A3	19990201		

AB A trench photosensor for use in a **CMOS** imager having an improved charge capacity. The trench photosensor may be either a photogate or photodiode structure. The trench shape of the photosensor provides the photosensitive element with an increased surface area compared to a flat photosensor occupying a comparable area on a substrate. The trench photosensor also exhibits a higher charge capacity, improved dynamic range, and a better signal-to-noise ratio. Also disclosed are processes for forming the trench photosensor.

RE.CNT 44 THERE ARE 44 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 5 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 2000:716130 CAPLUS
DN 133:275235
TI Bipolar **transistor** with L-shaped base-emitter spacer
IN Johnson, Frank S.; McAnally, Peter S.
PA Texas Instruments Incorporated, USA
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6130136	A	20001010	US 1998-196376	19981119

AB A method for fabricating a spacer in a bipolar **transistor**. The method comprises the steps of forming a stepped feature on the surface of a semiconductor material, the stepped feature having a lateral face substantially parallel to the surface and an angled face substantially perpendicular to the surface. An **insulating layer** is formed over the lateral and angled faces of the stepped feature and a sacrificial layer is formed over the **insulating layer** and over the lateral and angled faces of the stepped feature. The portion of the sacrificial layer over the lateral face is removed to expose portions of the **insulating layer** and to leave a portion of the sacrificial layer to cover the angled face of the stepped feature. Finally, the exposed portions of the **insulating layer** are removed to leave an L-shaped **insulator layer**, such as may be useful to insulate the base electrode from the emitter electrode in a bipolar **transistor**.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 6 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 2000:606834 CAPLUS
DN 133:186541
TI Planarization method for self-aligned contact process
IN Chien, Sun-chieh; Wu, Der-yuan; Chen, Kun-cho
PA United Microelectronics Corp., Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6110827	A	20000829	US 1996-655074	19960603
	TW 428244	B	20010401	TW 1996-85104463	19960415
PRAI	TW 1996-85104463	A	19960415		

AB A planarization method for self-aligned contact process which is suitable for use in DRAM processing. Prior to the formation of the bottom terminal layer of the capacitor, the substrate surface is first planarized, thus avoiding stringer effects and related bridging problems arising from an undulating surface profile, during subsequent etching of the defined pattern. Also according to the method of this invention, by covering the silicon substrate that has **MOS transistors** laid on top with first a deposition of an **oxide layer**, then an etch discriminatory layer, and finally a planarization layer, a substrate with a smooth, plane surface is obtained.

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 7 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 2000:506085 CAPLUS
DN 133:98136
TI Deep sub-0.1 .mu.m **CMOS** device and self-aligned pocket process for fabrication
IN Rodder, Mark S.
PA Texas Instruments Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6093610	A	20000725	US 1998-94978	19980616
PRAI US 1997-50112P	P	19970618		

AB A self-aligned pocket process for formation of **CMOS** devices and the devices by a sidewall doped overlayer to achieve deep sub-0.1 .mu.m **CMOS** with reduced gate length variation. The localized pocket results in reduced CJ. The method includes providing a semiconductor substrate and forming a gate electrode over the substrate sepd. from the substrate by an elec. insulator. A preferably elec. insulating sidewall material which contains a dopant of predetd. cond. type is formed over and either in contact with or spaced from the sidewalls of the gate electrode. The dopant is caused to migrate into the substrate beneath the sidewall material with some lateral movement to form a pocket of the predetd. cond. type in the substrate. A further sidewall can be added to the sidewall material after pocket formation. The sidewall material can be later removed. Drain extensions and/or source/drain regions are formed in the substrate of cond. type opposite the predetd. cond. type, with or without use of sidewalls as a mask to provide minimal overlap between the drain extensions and/or source/drain regions and the pocket.
RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 8 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 2000:472520 CAPLUS
DN 133:67378
TI Method of forming a **transistor** having thin doped semiconductor gate
IN Rodder, Mark Stephen
PA Texas Instruments Incorporated, USA
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6087248	A	20000711	US 1999-225878	19990105
PRAI	US 1998-70449P	P	19980105		

AB A method of forming a **transistor** is disclosed that comprises the step forming a gate **insulator layer** on an outer surface of the substrate. A 1st gate conductor layer is formed outwardly from the gate **insulator layer**. The 1st gate conductor layer is extremely thin. Dopants are introduced into the layer to render it conductive by using a diffusion source layer. The diffusion source layer is then removed and replaced by a 2nd gate conductor layer having low resistance. The layer can be used to form a T-gate structure, a flush gate, or a conventional gate structure.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L51 ANSWER 9 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 2002:596784 CAPLUS
TI Manufacture of crown-shaped capacitor in DRAM
IN Chen, Li-Ye; Liau, Ying-Ruei
PA Vanguard International Semiconductor Corporation, Taiwan
SO Taiwan, 27 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI TW 390020	B	20000511	TW 1998-87106330	19980424

AB A crown-shaped capacitor for a memory device is formed by using: (1) an important early polysilicon plug manuf. process, and (2) an etch barrier layer. At first, a third **insulating layer** and an etch barrier layer are formed on device structure and the substrate. A node contact hole is formed through the etch barrier layer 34 and the first **insulating layer**. A plug is formed for filling the node contact hole. Next, a planarizing layer is formed on the etch barrier layer and the plug 42. A crown hole is formed in the planarizing layer to expose the plug. A first polysilicon layer is deposited on the etch barrier layer, the plug, and the remaining first planarizing layer. A sacrificial layer is formed over the first polysilicon layer thereby filling the crown hole. The sacrificial layer and the first polysilicon layer are etched back to remove the exposed portions of the first polysilicon layer covered on the planarizing layer. The sacrificial layer is selectively removed thereby forming a crown-shaped storage electrode.

L51 ANSWER 11 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 1997:622943 CAPLUS
DN 127:286896
TI Manufacture of semiconductor **integrated circuit** and the **circuit** itself
IN Kikushima, Kenichi; Otsuka, Fumio; Nakamura, Morio
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 19 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 09246397	A2	19970919	JP 1996-51187	19960308

AB The title method involves forming side walls on the gate electrodes of n and p MOSs, selectively covering the walls with an anhyd. **insulator film**, selectively removing the walls having a water content with HF, selectively forming side walls on the gate electrodes, and forming the shallow regions of the MOSs by dopant diffusion from the side walls. A LDD structure is obtained without the adverse effects of implantation doping. A circuit manufd. by the above method is also described.

L51 ANSWER 12 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 1997:562610 CAPLUS
DN 127:241988
TI Semiconductor **integrated circuit** and its production
IN Hashimoto, Hisashi
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 09213940	A2	19970815	JP 1996-18670	19960205

AB A semiconductor **integrated circuit** having source and drain contacts selfaligned to its gate electrode comprises a substrate having step and planar regions and has contact holes in the **insulator films** on the step regions. The title method involves forming an **insulator film** on a substrate having step and planar regions and anisotropically etching the **insulator film** at the step regions to form the contact holes. Specifically, the **insulator film** may comprise PSG and Si nitride.

L51 ANSWER 13 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 1995:705757 CAPLUS
DN 123:158131
TI Source/drain structural configuration for MOSFET **integrated circuits** and fabrication of the circuits
IN Lur, Water
PA United Microelectronics Corp., Taiwan
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5428240	A	19950627	US 1994-271859	19940707

AB A source/drain structural configuration suitable for MOSFETs is provided, having a wedge-shaped configuration with a thickness that increases in the direction from its end near the channel of the **transistor** toward the other end. The source/drain configuration includes a shallow junction advantageously formed to reduce sheet resistance and prevent the hot carrier punchthrough effect. The wedge-shaped source/drain configuration is fabricated by depositing a **dielec. layer**, which is flowable under thermal treatment, after the formation of a polysilicon gate electrode. After annealing, the **dielec. layer** is etched to form a wedge-shaped mask. The resulting mask has a thickness that decreases in the direction from its end near the gate electrode toward the other end. The presence of the wedge-shaped shielding masks facilitates the formation of a pair of wedge-shaped source/drain regions on the substrate by implementation of an ion implantation procedure. The wedge-shaped mask also assists in achieving improved step coverage for the deposition of the pre-metal **dielec. layer**.

L51 ANSWER 14 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 1991:197917 CAPLUS
DN 114:197917
TI Manufacture of semiconductor device
IN Hayakawa, Kiyoharu; Sugiyama, Susumu; Takigawa, Mitsuharu
PA Toyota Central Research and Development Laboratories, Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 02304918	A2	19901218	JP 1989-126127	19890519

AB A method for manufg. a semiconductor device involves: (1) consecutively forming Si nitride, polycryst. Si, and interlayer **insulating films** on a semiconductor substrate having circuit elements; (2) etching only the interlayer **insulating film** to form an opening for a contact region; (3) etching only the polycryst. Si film in the opening; (4) heat-treating in steam to flow the interlayer **insulating film** for smoothing the contact hole, and to oxidize the polycryst. Si film; and (5) etching the remaining Si nitride film on the contact region. The interlayer **insulating film** may consist of **phosphosilicate** or borophosphosilicate glass. The method is useful for manufg. a **MOS transistor**

L51 ANSWER 15 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 1986:601546 CAPLUS
DN 105:201546
TI Semiconductor device
IN Aizawa, Takashi
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 61116859	A2	19860604	JP 1984-237912	19841112

AB A method for fabricating a semiconductor device (e.g., **MOS integrated circuit**) is described, which involves the prepn. of a 1st element(s) (e.g., **MOS** FET) having a high withstand voltage and a 2nd element(s) (e.g., **MOS** FET) which has a low withstand voltage and which is used for controlling the 1st element(s) on a semiconductor substrate. The method involves: (1) forming a stopper layer (e.g., Si3N4) on the substrate regions supporting the 1st element(s); (2) forming a high-concn. **phosphosilicate** glass film on all surfaces of the substrate; (3) removing the glass film on the substrate regions having the 1st element(s); and (4) forming a low-concn. **phosphosilicate** glass film on at least the substrate regions supporting the 1st element(s).

L51 ANSWER 16 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 1986:489702 CAPLUS
DN 105:89702
TI Semiconductor device
IN Kato, Masataka; Washio, Katsuyoshi
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 61058270	A2	19860325	JP 1984-178320	19840829

AB The radiation-resistant **integrated circuit** is prepd. by depositing a 200 .ANG. **oxide layer** and a 500 .ANG. **phosphosilicate** glass **insulating layer** on a **MOS transistor**. Holes are formed through the **oxide** and **insulating layers** near the source and drain regions, and electrodes are formed.

L51 ANSWER 17 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 1986:453115 CAPLUS
DN 105:53115
TI **Integrated circuit**
IN Kato, Yuri
PA Suwa Seikosha Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 61039516	A2	19860225	JP 1984-160404	19840730
	US 4669176	A	19870602	US 1985-756895	19850719
PRAI	JP 1984-160404		19840730		
	JP 1984-192301		19840913		

AB The metal contacts in MOSFETs in large-scale **integrated circuits** are formed by forming contact holes in an **insulating layer**, connecting the Si substrate and the n-type diffusion layer, and filling the hole with a refractory metal silicide. The silicide is coated with a P-doped Si compd. and annealing is performed briefly with a halogen lamp. The P-contg. coating is applied by spin-coating a **phosphosilicate** glass.

L51 ANSWER 18 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 1985:15140 CAPLUS
DN 102:15140
TI Mark for position matching
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 59121836	A2	19840714	JP 1982-227602	19821228
	JP 03055973	B4	19910827		

AB The prepn. of a mark for position matching involves the following: (1) forming an oxidn.-resistant film (e.g., SiO2 + Si3N4) having a desired shape on a semiconductor substrate (e.g., Si); (2) selectively oxidizing the exposed portions of the substrate to form an **oxide film**; (3) removing the oxidn.-resistant film; (3) forming an etch-resistant film (e.g., photoresist) on the overall surfaces excluding the unoxidized regions and portions of the **oxide film** surrounding the unoxidized regions; and (4) etching the substrate to produce a groovelike mark at the unoxidized regions of the substrate. Optionally, the etching-resistant film may consist of nondoped polycryst. Si and **phosphosilicate** glass films. The above prepn. steps are useful for the prepn. of a mark for electron-beam lithog. during the fabrication of an **integrated circuit**.

L51 ANSWER 19 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 1984:44043 CAPLUS
DN 100:44043
TI High-speed semiconductor device
PA Oki Electric Industry Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 58162061	A2	19830926	JP 1982-44633	19820323

AB High-speed **integrated-circuit MOS** devices are formed without loss of silicide by evapn. during the silicide oxidn. state by capping the silicide with an **oxide** and nitride **insulator layer** prior to oxidn. Thus, **Mo** silicide on Si was capped with SiO2 prior to oxidn. in **transistor** fabrication.

L51 ANSWER 20 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 1983:446682 CAPLUS
DN 99:46682
TI **Insulator films** for semiconductor device
PA Nippon Texas Instruments K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 58048938	A2	19830323	JP 1981-146375	19810918

AB The moisture resistance and disconnection characteristics of **MOS** devices for **integrated circuits** improved by coating the device with a soln. of H4SiO4 in alc. and heating at .apprx.1000.degree. to form a SiO2 layer.

L51 ANSWER 21 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 1983:208598 CAPLUS
DN 98:208598
TI Rounding off the interoxide between polysilicon and metal conductor planes in the preparation of integrated n-channel **MOS**-field effect **transistors**
IN Wichmann, Bernhard; Doering, Elko; Herbst, Jutta
PA Siemens A.-G. , Fed. Rep. Ger.
SO Ger. Offen., 8 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI DE 3133516	A1	19830317	DE 1981-3133516	19810825

AB A method for rounding-off the edges of the intermediate oxide between the poly-Si and metal conductor path planes consists of **coating** the intermediate **oxide** with a P silicate mixt. (contg. .ltoreq.5 wt. % P) from the thermal decompn. of SiH4 and PH3, heating this layer at .ltoreq.900.degree. to flow a **phosphosilicate** glass over the intermediate oxide, and opening contact holes.

L51 ANSWER 22 OF 22 CAPLUS COPYRIGHT 2002 ACS
AN 1984:16025 CAPLUS
DN 100:16025
TI Three-dimensional **CMOS** IC's fabricated by using beam recrystallization
AU Kawamura, S.; Sasaki, N.; Iwai, T.; Nakano, M.; Takagi, M.
CS IC Dev. Div., Fujitsu Ltd., Kawasaki, 211, Japan
SO IEEE Electron Device Lett. (1983), EDL-4(10), 366-8
CODEN: EDLEDZ; ISSN: 0193-8576
DT Journal
LA English
AB A 3-dimensional (3-.nu.) complementary **MOS integrated circuit** with a structure, in which one type of **transistor** is fabricated directly above a **transistor** of the opposite type with sep. gates and an insulator in between, was fabricated by using laser beam recrystn. Seven-stage ring oscillators fabricated in the 3-D structure have a propagation delay of 8.2 ns. A double-layer of Si3N4 and **phospho-silicate**-glass (PSG) film was used as an intermediate **insulating layer** between the top and the bottom devices. This **CMOS** structure and the process technol. can be the basis for realizing a multilayered 3-D device composed of vertically stacked **transistors** with sep. gates and an **insulating layer** in between.

13aug02 11:31:04 User267149 Session D276.1

SYSTEM:OS - DIALOG OneSearch
File 2:INSPEC 1969-2002/Aug W2
(c) 2002 Institution of Electrical Engineers
*File 2: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 6:NTIS 1964-2002/Aug W4
(c) 2002 NTIS, Intl Cpyrght All Rights Res
*File 6: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 8:Ei Compendex(R) 1970-2002/Aug W2
(c) 2002 Engineering Info. Inc.
*File 8: Alert feature enhanced for multiple files, duplicates removal, customized scheduling. See HELP ALERT.
File 34:SciSearch(R) Cited Ref Sci 1990-2002/Aug W2
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File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
(c) 1998 Inst for Sci Info
File 35:Dissertation Abs Online 1861-2002/Jul
(c) 2002 ProQuest Info&Learning
File 65:Inside Conferences 1993-2002/Aug W2
(c) 2002 BLDSC all rts. reserv.
File 77:Conference Papers Index 1973-2002/Jul
(c) 2002 Cambridge Sci Abs
File 94:JICST-EPlus 1985-2002/Jun W3
(c)2002 Japan Science and Tech Corp(JST)
*File 94: There is no data missing. UDs have been adjusted to reflect the current months data. See Help News94 for details.
File 99:Wilson Appl. Sci & Tech Abs 1983-2002/Jun
(c) 2002 The HW Wilson Co.
File 108:Aerospace Database 1962-2002/Jul
(c) 2002 Cambridge Sci Abs
File 144:Pascal 1973-2002/Aug W2
(c) 2002 INIST/CNRS
File 238:Abs. in New Tech & Eng. 1981-2002/Jul
(c) 2002 Cambridge Sci Abs
File 305:Analytical Abstracts 1980-2002/Jul W4
(c) 2002 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate removal, customized scheduling. See HELP ALERT.
File 315:ChemEng & Biotec Abs 1970-2002/Jun
(c) 2002 DECHEMA

13,087

08/13/2002 09/8[redacted]

Set	Items	Description
S1	746	AU=(BRYANT, F? OR BRYANT F?)
S2	14	S1 AND (INTEGRAT??????(3N)(CIRCUIT?????? OR LOOP? ?))
S3	10	S2 AND (MOS OR METAL()OXIDE(1W)SEMICONDUCT??????? OR NMOS? ? OR N()MOS? ? OR PMOS? ? OR P()MOS? ? OR VMOS? ? OR V()MOS? ? OR CMOS? ? OR C()MOS? ?)
S4	5	RD (unique items)
S5	13	S1 AND (MOS OR METAL()OXIDE(1W)SEMICONDUCT??????? OR NMOS? ? OR N()MOS? ? OR PMOS? ? OR P()MOS? ? OR VMOS? ? OR V()MOS? ? OR CMOS? ? OR C()MOS? ?)
S6	8	S5 NOT S4
S7	4	RD (unique items)
S8	0	S1 AND (PRINTHEAD? ? OR PRINT()HEAD? ?)
S9	57	AU=(TORGERSON, J? OR TORGERSON J)
S10	0	S9 AND (PRINTHEAD? ? OR PRINT()HEAD? ?)
S11	0	S9 AND (MOS OR METAL()OXIDE(1W)SEMICONDUCT??????? OR NMOS? ? OR N()MOS? ? OR PMOS? ? OR P()MOS? ? OR VMOS? ? OR V()MOS? ? OR CMOS? ? OR C()MOS? ?)
S12	0	S9 AND (INTEGRAT??????(3N)(CIRCUIT?????? OR LOOP? ?))
S13	0	AU=(BAKKOM,A? OR BAKKOM A)
S14	4	S2 NOT S3
S15	3	RD (unique items)

08/13/2002 09/813,087

13aug02 12:48:35 User267149 Session D277.1

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removal, customized scheduling. See HELP ALERT.
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         (c) 2002 NTIS, Intl Cpyrght All Rights Res
*File   6: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
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         (c) 2002 Engineering Info. Inc.
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removal, customized scheduling. See HELP ALERT.
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         (c) 2002 Inst for Sci Info
*File  34: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
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         (c) 1998 Inst for Sci Info
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         (c) 2002 ProQuest Info&Learning
  File  65:Inside Conferences  1993-2002/Aug W2
         (c) 2002 BLDSC all rts. reserv.
  File  77:Conference Papers Index  1973-2002/Jul
         (c) 2002 Cambridge Sci Abs
  File  94:JICST-EPlus  1985-2002/Jun W3
         (c)2002 Japan Science and Tech Corp(JST)
*File  94: There is no data missing. UDs have been adjusted to reflect
 the current months data. See Help News94 for details.
  File  99:Wilson Appl. Sci & Tech Abs  1983-2002/Jun
         (c) 2002 The HW Wilson Co.
  File 108:Aerospace Database  1962-2002/Jul
         (c) 2002 Cambridge Sci Abs
  File 144:Pascal  1973-2002/Aug W2
         (c) 2002 INIST/CNRS
  File 238:Abs. in New Tech & Eng.  1981-2002/Jul
         (c) 2002 Cambridge Sci Abs
  File 305:Analytical Abstracts  1980-2002/Jul W4
         (c) 2002 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2002/Jun
         (c) 2002 DECHEMA
  File 350:Derwent WPIX  1963-2002/UD,UM &UP=200251
         (c) 2002  Thomson Derwent
*File 350: Alerts can now have images sent via all delivery methods.
See HELP ALERT and HELP PRINT for more info.
  File 347:JAPIO  Oct 1976-2002/Apr(Updated 020805)
         (c) 2002 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs  Aug 1985-2002/Aug
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*File 371: This file is not currently updating. The last update is 200209.

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S1     408049   MOS OR METAL()OXIDE(1W)SEMICONDUCT??????? OR NMOS? ?  OR N-
           ()MOS? ? OR PMOS? ? OR P()MOS? ? OR VMOS? ? OR V()MOS? ? OR C-
           MOS? ? OR C()MOS? ?
S2     233775   MOSFET? ? OR MOS()FET? ? OR METAL()OXIDE(1W)SEMICONDUCT???-
           ??
S3     176568   FIELD()EFFECT? ?(1W)TRANSIST??????? OR FET
S4      27764   CC=B2560R  Insulated gate field effect transistors
S5       4951   MC=S01-G02B
S6      23893   IC=(G01R-031/26 OR G01R-031/27)
S7     612498   S1:S6
S8    6682281   CIRCUIT?????? OR LOOP? ? OR PATH? ? OR ROUTE? ? OR ELECTRO-
           DE? ?
S9     640301   INTEGRAT??????(3N)(CIRCUIT?????? OR LOOP? ?)
S10    190511   CLOS??????(3N)(CIRCUIT?????? OR LOOP? ? OR PATH? ? OR ROUT-
           E? ? OR ELECTRODE? ?)
S11     21839   MC=(U11-D01A OR U13-D02 OR U13-D02A)
S12     37847   IC=(H01L-023/12 OR H01L-027/085 OR H01L-027/088 OR H01L-02-
           7/092)
S13     73135   CC=(B2220 OR B2570)
S14   6714059   S8:S13
S15   2225899   FLUID? ? OR LIQUID? ?()JET? ?  OR FLUIDJET? ?
S16     97761   INKJET? ? OR INK()JET? ? OR INK()JETT??? OR INKJETT???
S17    145367   IC=(B41J-002 OR G06K-015)
S18     16402   MC=T04-G02
S19    191801   S16:S18
S20   1923975   SUBSTRATE? ?
S21    618106   TRANSISTOR? ?
S22    220388   CARRIAGE? ?  OR CARTRIDGE? ?
S23      2340   (FLUID? ? OR LIQUID? ?)(3N)(CARRIAGE? ?  OR CARTRIDGE? ?)
S24     52227   (FLUID? ? OR LIQUID? ?)(3N)(RESERVOIR? ? OR CHANNEL??????)
S25    125965   RECORD??????(3N)DEVICE? ?
S26    114200   (PRESSUR?????? OR COMPRESS??????)(3N)(REGULAT?????? OR CON-
           TROL ?????? OR DIRECT??????)
S27    231499   AIR(3N)(PRESSUR?????? OR COMPRESS??????)
S28    334626   S26:S27
S29      1547   EJECT??????(3N)ELEMENT? ?
S30    718146   (INSULAT?????? OR OXIDE? ? OR DIELECTRIC???)(3N)(LAYER??? -
           OR FILM??? OR COAT??? OR MULTILAYER??? OR SPACER???)
S31     12684   MC=(U11-C06A1B OR U11-C07C3 OR U11-C08A1 OR U11-C08A6)
S32     27805   CC=(A5150 OR A7700 OR B2800 OR B2810 OR B2830)
S33    748925   S30:S32
S34      3131   (PHOSPHOSILICATE OR PHOSPHO()SILICATE)(3N)GLASS
S35     32695   THERMAL??????(3N)OXIDE? ?
S36    510382   (SILICON()DIOXIDE) OR SI02 OR QUARTZ OR (SILICON()NITRIDE)
           OR SIN OR (SILICON()CARBIDE) OR CARBOLON OR CARBORUNDUM
S37   6437481   TANTALUM OR TA OR ALUMINIUM OR AL OR COPPER OR CU OR GOLD -
           OR AU OR TUNGSTEN OR W OR MOLYBDENUM OR MO
S38   6841468   S36:S37
S39    272111   S22:S24
S40    373886   S7 AND S14
S41     17874   (PRINTHEAD? ? OR PRINT()HEAD? ?)
S42       140   S40 AND S41
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S43	94	S42 AND S19
S44	1	S43 AND S13
S45	93	S43 NOT S44
S46	24	S45 AND S20
S47	10	S46 AND S21
S48	10	RD (unique items)
S49	1	S48 AND S22
S50	9	S48 NOT S49
S51	0	S50 AND S39
S52	0	S50 AND S28
S53	14	S46 NOT S48
S54	0	S53 AND S22
S55	0	S53 AND S39
S56	0	S53 AND S28
S57	2	S53 AND S33
S58	81	S45 NOT S48,S57
S59	6	S58 AND S38
S60	6	RD (unique items)
S61	75	S58 NOT S60
S62	0	S61 AND (S34 OR S35)
S63	1	S61 AND S25
S64	74	S61 NOT S63
S65	2	S6 AND S41
S66	934	S6 AND S38
S67	3	S66 AND (S34 OR S35)
S68	3	RD (unique items)
S69	931	S66 NOT S68
S70	500	S69 AND S14
S71	0	S70 AND S25
S72	8	S70 AND (S15 OR S19 OR S39)
S73	8	RD (unique items)
S74	492	S70 NOT S73
S75	38	S74 AND S1
S76	12	S75 AND S9
S77	0	S76 AND S19
S78	5	S76 AND (S20 OR S21)
S79	5	RD (unique items)
S80	7	S76 NOT S79
S81	0	S80 AND S29
S82	480	S74 NOT S76
S83	0	S82 AND S41
S84	37	S82 AND PRINT???????
S85	0	S84 AND S19
S86	0	S84 AND (S15 OR S39)
S87	7	S84 AND S33
S88	7	RD (unique items)
S89	30	S84 NOT S88
S90	0	S89 AND S22
S91	30	S89 AND S14
S92	0	S91 AND S1
S93	0	S91 AND S2
S94	0	S91 AND S3
S95	30	S91 AND (S4-S6)
S96	0	S95 AND S34

S97	30	S95 AND S38
S98	30	RD (unique items)
S99	0	S97 AND S15
S100	0	S97 AND S34
S101	0	S97 AND (PHOSPHOSILICATE OR PHOSPHO()SILICATE)
S102	623380	S14 AND S38
S103	2213	S102 AND S19
S104	218	S103 AND S41
S105	105	S104 AND (S20 OR S21)
S106	7	S105 AND S15
S107	7	RD (unique items)
S108	98	S105 NOT S107
S109	1	S108 AND S28

44/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7218612 INSPEC Abstract Number: B2002-04-2570-011, C2002-04-5550-005
Title: High resolution long array thermal **ink jet printhead** with on-chip LSI heater plate and micromachined Si channel plate
Author(s): Murata, M.; Kataoka, M.; Nayve, R.; Fukugawa, A.; Ueda, Y.; Mihara, T.; Fujii, M.; Iwamori, T.
Author Affiliation: Ink Jet Bus. Unit, Fuji Xerox Co. Ltd., Ebina-shi, Japan
Journal: IEICE Transactions on Electronics vol.E84-C, no.12 p. 1792-800
Publisher: Inst. Electron. Inf. & Commun. Eng,
Publication Date: Dec. 2001 Country of Publication: Japan
CODEN: IELEEJ ISSN: 0916-8524
SICI: 0916-8524(200112)E84C:12L.1792:HRLA;1-0
Material Identity Number: P712-2002-001
Language: English
Abstract: This paper presents a high resolution long array thermal **ink jet** (TIJ) **printhead** which has been developed and demonstrated to operate successfully by combining two functional Si wafers, a bubble generating heater plate fabricated using LSI processes and a channel plate fabricated using Si bulk micromachining technology. The heater plate consists of logic LSIs, high voltage **MOS** transistor, polycrystalline Si (poly Si) heating resistor and polyimide protective layer. The polymide layer is patterned by O/sub 2/ plasma reactive ion etching (RIE) and is applicable to high resolution heater array. The Si channel plate consists of an ink chamber and an ink inlet formed by KOH etching, and a nozzle formed by inductively coupled plasma RIE (ICP RIE). The nozzle formed by RIE has squeezed structures which contribute to high energy efficiency of the drop ejector and therefore successful ejection of small ink drop. These two wafers are directly bonded by novel electrostatic bonding of full-cured polyimide to Si. The adhesive-less bonding provided an ideal shaped small nozzle orifice. Also, the bonding method enabled use of an on-chip LSI wafer because of the contamination free material and the suitable processing conditions (low temperature). The bonded wafer is diced to form the **printhead** chip. No delamination or displacement of the chip was observed even though the chip was subjected to thermal stress during assembly. This is because there is no difference in thermal expansion coefficient between the chips (Si and Si), and therefore it is suitable for the long chip concept. With these technologies, we have fabricated a 1.3'' long **printhead** with 1024 nozzles having a 800 dots per inch (dpi) resolution, a 2.7 pl. ink drop volume, 14 m/s ink drop velocity and 18 kHz jetting frequency, and we have confirmed high speed and high quality printing.
Subfile: B C

49/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009659750
WPI Acc No: 1993-353301/199345
XRPX Acc No: N93-272511
Electrostatic discharge protection **circuit** for **integrated circuit** esp. HV power i.e. over 25V input terminals. - has electrostatic discharge protection **transistor** connected, in parallel with power **MOS** driver, to high voltage input terminal, and operates with lateral bipolar action
Patent Assignee: XEROX CORP (XERO)
Inventor: HAWKINS W G
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 569219	A2	19931110	EP 93303468	A	19930504	199345	B
JP 6021343	A	19940128	JP 93101701	A	19930428	199409	
US 5371395	A	19941206	US 92879626	A	19920506	199503	
EP 569219	A3	19951108	EP 93303468	A	19930504	199617	
EP 569219	B1	19980610	EP 93303468	A	19930504	199827	
DE 69319021	E	19980716	DE 619021	A	19930504	199834	
			EP 93303468	A	19930504		

Priority Applications (No Type Date): US 92879626 A 19920506
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 569219	A2	E	21	H01L-027/02	
Designated States (Regional): DE FR GB					
US 5371395	A		18	H01L-023/62	
EP 569219	B1	E		H01L-027/02	
Designated States (Regional): DE FR GB					
DE 69319021	E			H01L-027/02	Based on patent EP 569219
JP 6021343	A			H01L-027/04	
EP 569219	A3			H01L-027/02	

Abstract (Basic): EP 569219 A

The ESD **circuit** protects a semiconductor device formed on a silicon **substrate** (20), which is connected to a HV terminal. The ESD protection **circuit** is formed in the same **substrate** and has a diffused drain region (68) connected to the HV input terminal, a second source diffusion region (70) connected to ground, a field oxide layer (66) over the **substrate** with a thickened region (66a) extending into the **substrate** between the two diffusion regions, and a drift region (78) between the drain and the thickened field oxide layer, under which there is a channel stop (72) region.

The breakdown voltage of the semiconductor device is greater than the breakdown voltage of the ESD protection device and the ESD hardness of the ESD protection device is greater than the ESD hardness of the semiconductor device.

USE - Power **MOSFET** esp. in customer replaceable **printhead** or print **cartridge** of e.g thermal **ink-jet** printer.

Dwg.6c/8

Abstract (Equivalent): US 5371395 A

The overvoltage protection structure protecting a high voltage operating **circuit** having a high voltage input terminal has an N+ diffusion region in a lightly doped P region of a silicon **substrate** and connected to the high voltage input terminal formed on the **substrate**. A P+ diffusion region formed in the **substrate** is connected to ground. There is a moderately doped P region in the lightly doped P region between the N+ and P+ diffusions and adjacent the P+ diffusion.

A field oxide layer over the **substrate** has a thickened region extending into the **substrate** between the P+ and N+ diffusions. An N- drift region is located in the **substrate** between the N+ diffusion and moderately doped P region. The regions are arranged to move the point of avalanche breakdown away from the N+ diffusion/field oxide interface, so that the avalanche breakdown voltage is lower than that of the protected **circuit**.

USE/ADVANTAGE - In customer replaceable **printhead** or print **cartridge** e.g. in thermal **ink-jet** printer; ESD protection. Simultaneously preventing avalanche included bipolar feedback in protection device; low input pad impedance.

Dwg.6c/8

48/3,AB/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04305037
E.I. No: EIP95122952200
Title: Even smaller and faster devices at 41st IEDM
Author: Anon
Source: IEEE Circuits and Devices Magazine v 11 n 6 Nov 1995. p 17-20
Publication Year: 1995
CODEN: ICDMEN ISSN: 8755-3996
Language: English
Abstract: The upcoming IEFE International Electron Devices Meeting (December 10-13, 1995, Washington D.C.) is characterized by an anticipation of the coming developments in the industry. Among the highlights include the fastest silicon-based **transistor** ever built, the effort towards building a 1-gigabit DRAM memory chip, including the smallest memory cell ever reported, and the integration of **inkjet printheads**, optical fiber, and test probe tips with electronics on common **substrates**.

48/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014303301
WPI Acc No: 2002-124004/200217
XRPX Acc No: N02-093035
Printhead for printer, controls terminal-to-terminal potential difference of printing element to be equal to voltage of constant voltage source, when printing element is driven
Patent Assignee: CANON KK (CANO); HIRAYAMA N (HIRA-I)
Inventor: HIRAYAMA N
Number of Countries: 028 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1142715	A1	20011010	EP 2001303163	A	20010403	200217	B
US 20010045968	A1	20011129	US 2001822193	A	20010402	200217	
JP 2001277516	A	20011009	JP 2000101481	A	20000403	200217	

Priority Applications (No Type Date): JP 2000101481 A 20000403
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1142715	A1	E	18	B41J-002/05	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
US 20010045968	A1			B41J-029/38	
JP 2001277516	A		10	B41J-002/05	

Abstract (Basic): EP 1142715 A1
Abstract (Basic):
NOVELTY - A **metal oxide semiconductor** (**MOS**) **transistor** (21) connected in series with a printing element, controls driving of the printing element with voltage applied to a control terminal. A voltage controlled **circuit** controls terminal-to-terminal potential difference of the printing element to be equal to a voltage of a constant voltage source (VR1), when the printing element is driven.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Printer;

(b) **Printhead substrate**;

(c) **Printhead** control **circuit**

USE - For printers such as **inkjet** printers for information providing apparatus such as word processor, personal computer, facsimile, copier.

ADVANTAGE - Suppresses influence of changes in power supply voltage and wiring resistance of a power supply line, and keeps drive conditions equal on each printing element, therefore, high image quality is provided and cost for power supply apparatus and wiring is reduced. Maintains storage quality, since each printing element is driven under constant conditions regardless of changes in characteristics of internal element due to temperature changes of the **printhead**.

48/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014213796
WPI Acc No: 2002-034494/200204
XRAM Acc No: C02-009692
XRPX Acc No: N02-026541
Inkjet printhead for high-resolution and high-speed printing comprises **substrate**, nozzle(s), drive mechanism, and electrical devices
Patent Assignee: KOREA ADV INST SCI & TECHNOLOGY (KOAD); CHUN K (CHUN-I); HAN C (HANC-I); LEE C (LEEC-I); LEE J (LEEJ-I)
Inventor: CHUN G C; HAN C H; LEE C S; LEE J D; CHUN K C; CHUN K; HAN C; LEE C; LEE J
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200183220	A1	20011108	WO 2000KR584	A	20000605	200204	B
US 20010040596	A1	20011115	US 2000729269	A	20001205	200204	
KR 2001102636	A	20011116	KR 200023620	A	20000503	200231	

Priority Applications (No Type Date): KR 200023620 A 20000503
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200183220	A1	E	30	B41J-002/235	
Designated States (National): JP					
US 20010040596	A1			B41J-002/145	
KR 2001102636	A			B41J-002/145	

Abstract (Basic): WO 200183220 A1
Abstract (Basic):
NOVELTY - An **inkjet printhead** comprises a **substrate** having at least four ink-supply **path** orifices arranged in a two-dimensional array, nozzle(s) (12') connected to each orifice, a drive mechanism for driving the nozzle, and electrical devices for decoding electric signals provided from outside the **printhead** and transmitting the signals to the driving mechanism to drive the nozzle.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of fabricating an **inkjet printhead** comprising sequentially forming a silicon oxide layer and a silicon nitride layer on a silicon **substrate** (10) doped with a first conductivity-type impurity; etching the silicon oxide layer and the silicon nitride layer except in a switching device area and a main ink-supply **path** (15) area to expose parts of the **substrate**; doping the exposed parts with a second conductive-type impurity; oxidizing the exposed parts to form a heat-transfer-prevention silicon oxide layer on the exposed parts of the **substrate**; removing the silicon oxide layer and the silicon nitride layer over the entire main ink-supply **path** area and on both ends of the switching device area; doping the entire main ink-supply **path** area and both ends of the switching device area with the first conductive-type impurity to form a device-separation

first conductive-type impurity diffusion layer; sequentially carrying out oxidizing and heat treating processes to reduce the doping concentration of the device-separation silicon oxide layer at both ends of the switching device area and make the heat-transfer-prevention silicon oxide layer thicker; removing the remaining silicon nitride layer and the silicon oxide layer under the silicon nitride layer; forming on the switching device area, a switching **transistor** including a gate oxide layer, a polysilicon gate **electrode** layer, and a source-drain area; removing the oxide layer on the main ink-supply **path** area and carrying out a doping process with the first conductive-type impurity to reduce a contact resistance between the main ink-supply **path** area and a metal wiring to be formed subsequently; removing the oxide layer on the source-drain area and depositing and etching the metal wiring and a heater resistor (16) film to form wiring and the heater resistor, sequentially depositing first and second passivation layers for protection of the **transistor**, the heater resistor, and the wiring from ink; etching the second passivation layer except in an area near the heater resistor; etching the first passivation layer on a pad-wiring contact window area and the main ink-supply **path** area; depositing a base metal layer for plating of a nozzle; forming a plating mold including an ink channel (14') mold, an ink chamber (13) mold, and a nozzle mold by photoresistor layer patterning for plating of the nozzle plate (11); forming the nozzle plate by plating using the plating mold, the thickness of plating being less than the height of the photoresistor layer; and removing the plating mold and subsequently removing the base metal layer.

USE - For high-resolution and high-speed printing.

ADVANTAGE - The device improves printing capability, and can be operated at high speed and high resolution.

DESCRIPTION OF DRAWING(S) - The figure shows a perspective view of the **inkjet printhead** integrated on a silicon **substrate**.

Silicon **substrate** (10)
Nozzle plate (11)
Nozzle (12')
Ink chamber (13)

48/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013274400
WPI Acc No: 2000-446320/200039
XRPX Acc No: N00-333224
Print head drive control **integrated circuit** includes operational amplifier with P-type and N-type **metal oxide semiconductor transistor** of different sizes
Patent Assignee: SANYO ELECTRIC CO LTD (SAOL)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000158700	A	20000613	JP 98337851	A	19981127	200039	B

Priority Applications (No Type Date): JP 98337851 A 19981127
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000158700	A		4	B41J-002/44	

Abstract (Basic): JP 2000158700 A
Abstract (Basic):
NOVELTY - The **integrated circuit** consists of a constant current **circuit** with a operational amplifier (5) having final stage as inversion amplification stage with P-type and N-type **MOS transistors** fabricated on a single semiconductor **substrate**. According to the polarity, either the size of P-type or N-type is made larger.
USE - Used for **print head** drive control.
ADVANTAGE - Since the size of any one of the **transistors** is increased, the noise generated by operational amplifier and the gain of the power consumption are suppressed, thereby reducing the printing irregularities.
DESCRIPTION OF DRAWING(S) - The figure shows the **circuit** diagram of the principal part of **print head** drive control **integrated circuit**.
Operational amplifier (5)
pp; 4 DwgNo 2/4

48/3,AB/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009989710
WPI Acc No: 1994-257421/199432
XRPX Acc No: N99-436236
Thermal **ink-jet print head** with power MOST driver giving enhanced transconductance - has increased breakdown voltage and reduced dimensions because of higher drift domain doping
Patent Assignee: XEROX CORP (XERO)
Inventor: BURKE C J; HAWKINS W G
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6143574	A	19940524	JP 93161863	A	19930630	199432	B
US 5969392	A	19991019	US 92971873	A	19921105	199951	
			US 94344397	A	19941123		

Priority Applications (No Type Date): US 92971873 A 19921105; US 94344397 A 19941123
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6143574	A		12	B41J-002/045	
US 5969392	A		16	H01L-029/76	Cont of application US 92971873

Abstract (Basic): US 5969392 A
Abstract (Basic):
NOVELTY - A single polysilicon layer (153) having a predetermined thickness and resistivity is formed on the insulative layers of a **substrate**. The polysilicon layer includes a polysilicon field plate portion and a gate portion which subtend a drift oxide and a gate oxide to function as a field plate (152) and a gate (128), respectively.
DETAILED DESCRIPTION - A drain region, comprising a drift region (150) and a contact region, (154) and a source region (155) are formed on the silicon **substrate** (146). Drift oxide and gate oxide layers (151,126) are adjacently formed on drift and channel regions. Aluminum contacts (142) are connected to the contact and source regions.
USE - For the **print head** of a drop-on-demand thermal **ink jet** printer.
ADVANTAGE - Influences the drift region to provide a less resistive drift region which is depleted of carriers, thus the transconductance of the **transistor** is increased without reducing the breakdown voltage. Increases current flow between the source and drain under high gate bias due to the single layer of uniformly doped polysilicon which serves as both a gate and a field plate.
DESCRIPTION OF DRAWING(S) - The figure shows an enlarged view of the **MOS** driver **circuit**.
Gate oxide layer (126)
Gate (128)
Aluminum contact (142)
Silicon **substrate** (146)

Drift region (150)
Drift oxide layer (151)
Field plate (152)
Polysilicon layer (153)

48/3,AB/6 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009713730
WPI Acc No: 1993-407283/199351
XRPX Acc No: N93-315250
Semiconductor device driver for heater in **ink-jet** or thermal **print head** - includes **MOS transistor** with buried drain and high resistance region between drain and channel surrounding source **electrode**
Patent Assignee: CANON KK (CANO)
Inventor: FUJITA K; ICHISE T; KAIZU S; KAMEI S; NAKAMURA H
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 574911	A2	19931222	EP 93109690	A	19930617	199351	B
JP 6069497	A	19940311	JP 93130289	A	19930601	199415	
EP 574911	A3	19940330	EP 93109690	A	19930617	199521	
US 5517224	A	19960514	US 9377382	A	19930617	199625	
EP 574911	B1	19990303	EP 93109690	A	19930617	199913	
DE 69323655	E	19990408	DE 623655	A	19930617	199920	
			EP 93109690	A	19930617		

Priority Applications (No Type Date): JP 93130289 A 19930601; JP 92159748 A 19920618
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 574911	A2	E	36	H01L-029/784	
Designated States (Regional): DE FR GB					
US 5517224	A		32	B41J-002/05	
EP 574911	B1	E		H01L-029/772	
Designated States (Regional): DE FR GB					
DE 69323655	E			H01L-029/772	Based on patent EP 574911
JP 6069497	A			H01L-029/784	
EP 574911	A3			H01L-029/784	

Abstract (Basic): EP 574911 A
The device includes a number of **MOS transistors**, forming a switching **circuit**. Each **transistor** includes a drain **electrode** with a high resistance region in contact with an opposite conductivity channel region. A source **electrode** is formed in the opposite conductivity region. A gate **electrode** is located on a gate insulating film between the two **electrodes**.
An n-type buried layer (201), formed on a silicon **substrate** (200), is beneath a p-type epitaxial layer (202). A contact layer (205) connecting to an n-type drain (204) is formed around an n-type epitaxial layer (203) on the edge of the buried layer. A p-layer (206) channel contains a p-type layer (207) and n-type sources (208, 209) on both sides of the p-type layer.
USE/ADVANTAGE - In e.g copier, facsimile. Short **circuited** junction element isolation structure to prevent latch-up; reduced

electric field strength, due to increased junction depth and wider depletion layer for increased voltage resistance.
Dwg.4/26

Abstract (Equivalent): US 5517224 A

A semiconductor device comprising:
a plurality of **transistors**, wherein each **transistor** comprises:
a first semiconductor region of a first conduction type, including a first main **electrode** region;
a second semiconductor region of a second conduction type, including a channel region, said second semiconductor region being disposed in said first semiconductor region and in contact therewith, said channel region being in contact with a portion of said first main **electrode** region;
a second main **electrode** region of the first conducting type disposed in said second semiconductor region and in contact with said channel region;
a gate insulating film disposed on said channel region;
a gate **electrode** disposed on said gate insulting film and in alignment with said channel region; wherein
said portion of said first main **electrode** region which contacts said channel region is a high-resistance region.
Dwg.10/26

48/3,AB/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009659750
WPI Acc No: 1993-353301/199345
XRPX Acc No: N93-272511
Electrostatic discharge protection **circuit** for **integrated circuit** esp. HV power i.e. over 25V input terminals. - has electrostatic discharge protection **transistor** connected, in parallel with power **MOS** driver, to high voltage input terminal, and operates with lateral bipolar action
Patent Assignee: XEROX CORP (XERO)
Inventor: HAWKINS W G
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 569219	A2	19931110	EP 93303468	A	19930504	199345	B
JP 6021343	A	19940128	JP 93101701	A	19930428	199409	
US 5371395	A	19941206	US 92879626	A	19920506	199503	
EP 569219	A3	19951108	EP 93303468	A	19930504	199617	
EP 569219	B1	19980610	EP 93303468	A	19930504	199827	
DE 69319021	E	19980716	DE 619021	A	19930504	199834	
			EP 93303468	A	19930504		

Priority Applications (No Type Date): US 92879626 A 19920506
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 569219	A2	E	21	H01L-027/02	
Designated States (Regional): DE FR GB					
US 5371395	A		18	H01L-023/62	
EP 569219	B1	E		H01L-027/02	
Designated States (Regional): DE FR GB					
DE 69319021	E			H01L-027/02	Based on patent EP 569219
JP 6021343	A			H01L-027/04	
EP 569219	A3			H01L-027/02	

Abstract (Basic): EP 569219 A
The ESD **circuit** protects a semiconductor device formed on a silicon **substrate** (20), which is connected to a HV terminal. The ESD protection **circuit** is formed in the same **substrate** and has a diffused drain region (68) connected to the HV input terminal, a second source diffusion region (70) connected to ground, a field oxide layer (66) over the **substrate** with a thickened region (66a) extending into the **substrate** between the two diffusion regions, and a drift region (78) between the drain and the thickened field oxide layer, under which there is a channel stop (72) region.
The breakdown voltage of the semiconductor device is greater than the breakdown voltage of the ESD protection device and the ESD hardness of the ESD protection device is greater than the ESD hardness of the semiconductor device.
USE - Power **MOSFET** esp. in customer replaceable **printhead** or print cartridge of e.g thermal **ink-jet**

printer.
Dwg.6c/8

Abstract (Equivalent): US 5371395 A
The overvoltage protection structure
protecting a high voltage operating **circuit** having a high voltage input terminal
has an N+ diffusion region in a lightly doped P region of a silicon **substrate** and connected to the high voltage input terminal formed on the **substrate**. A P+ diffusion region formed in the **substrate** is connected to ground. There is a moderately doped P region in the lightly doped P region between the N+ and P+ diffusions and adjacent the P+ diffusion.
A field oxide layer over the **substrate** has a thickened region extending into the **substrate** between the P+ and N+ diffusions. An N- drift region is located in the **substrate** between the N+ diffusion and moderately doped P region. The regions are arranged to move the point of avalanche breakdown away from the N+ diffusion/field oxide interface, so that the avalanche breakdown voltage is lower than that of the protected **circuit**.
USE/ADVANTAGE - In customer replaceable **printhead** or print cartridge e.g. in thermal **ink-jet** printer; ESD protection. Simultaneously preventing avalanche included bipolar feedback in protection device; low input pad impedance.
Dwg.6c/8

48/3,AB/8 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009254080
WPI Acc No: 1992-381497/199246
XRPX Acc No: N92-290940
Thermal **ink jet print-head** structure with integrated **MOSFET** drive **transistor** - forms dual-layer **MOSFET** structure by applying silicon dioxide and silicon nitride layers on silicon@ **substrate**, nitride layer partially removed to form reduced size structure surrounded by exposed silicon dioxide
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: BECKMANN J E; FASEN D A; HESS U E; HULINGS J R; METZ L S; MOORE C E; STANBACK J H
Number of Countries: 006 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5159353	A	19921027	US 91724658	A	19910702	199246	B
EP 521634	A2	19930107	EP 92305554	A	19920617	199301	
JP 5185598	A	19930727	JP 92199302	A	19920702	199334	
EP 521634	A3	19930512	EP 92305554	A	19920617	199402	
EP 521634	B1	19960424	EP 92305554	A	19920617	199621	
DE 69210115	E	19960530	DE 610115	A	19920617	199627	
			EP 92305554	A	19920617		
JP 3262595	B2	20020304	JP 92199302	A	19920702	200219	

Priority Applications (No Type Date): US 91724658 A 19910702
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5159353	A		17	B41J-002/05	
EP 521634	A2	E	19	B41J-002/16	
Designated States (Regional): DE FR GB IT					
JP 5185598	A			B41J-002/16	
EP 521634	A3			B41J-002/05	
EP 521634	B1	E	19	B41J-002/16	
Designated States (Regional): DE FR GB IT					
DE 69210115	E			B41J-002/16	Based on patent EP 521634
JP 3262595	B2		12	B41J-002/16	Previous Publ. patent JP 5185598

Abstract (Basic): US 5159353 A
The improved thermal **inkjet printhead** having **MOSFET** drive **transistors** incorporated therein. The gate of each **MOSFET transistor** is formed by applying a layer of silicon dioxide onto a silicon **substrate**, applying a layer of silicon nitride onto the silicon dioxide, and applying a layer of polycrystalline silicon onto the silicon nitride. Portions of the **substrate** surrounding the gate are oxids, forming field oxide regions. Drain and source regions are then conventionally formed, followed by the application of a protective dielectric layer onto the field oxide, drain, source, and gate.
A resistive layer is deposited on the dielectric layer and directly conneted to the source, drain, and gate. A conductive layer is

deposited on a portion of the resistive layer, ultimately forming both convered and uncovered regions of it. The uncovered region functions as a heating resistor, and the covered regions function as electrical contacts to the **transistor** and resistor.

ADVANTAGE - Improves **printhead** with **integrated** **MOSFET** drive **circuiting** has reduced number of processing steps over previous prodn. procedures. Highly efficient, economical, and lower prodn. costs.

Dwg.19/19

Abstract (Equivalent): EP 521634 B

A thermal **inkjet printhead** apparatus having at least one **MOSFET transistor** (126) positioned on said **substrate** (70), said **transistor** (126) comprising a source region (118), a drain region (120), and a gate (110) positioned between said source region (118) and said drain region (120), said gate (110) comprising: a layer (72) of silicon dioxide on said **substrate** (70); a layer of silicon nitride (76) on said layer (72) of silicon dioxide; and a layer (90) of polycrystalline silicon on said layer (76) of silicon nitride; a field oxide layer (84,86) on said **substrate** (70), said field oxide layer (84,86) on said **substrate** (70), said field oxide layer (84,86) surrounding said **transistor** (126) and being comprised of silicon dioxide; a layer (124) of dielectric material covering said field oxide layer (84,86) and said **transistor** (126), said layer (124) of dielectric material having a plurality of openings (174,176,177) therethrough, said openings (174,176,177) providing access to said source region (118), said drain region (120), and said gate (110) of said **transistor** (126); a layer (180) of electrically resistive material positioned on said layer (124) of dielectric material, said layer of electrically resistive material (180) being in direct electrical contact with said source region (118), said drain region (120), and said gate (110) through said openings (174,176,177); a layer (181) of conductive material affixed to a portion of said layer (180) of electrically resistive material in order to form a multi-layer structure (182), said layer (180) of electrically resistive material in said multi-layer structure (182) having at least one uncovered section (202) wherein said layer (181) of conductive material is absent therefrom, said uncovered section (202) functioning as a heating resistor (209); said layer (180) of electrically resistive material being covered with said layer (181) of conductive material at said source region (118), said drain region (120), and said gate (110) of said **transistor** (126); a portion (220) of protective material positioned on said heating resistor (209); and a plate member (240) having at least one opening (242) therethrough, said plate member (240) being secured to said portion (220) of protective material, said portion (220) of protective material having a section thereof removed directly beneath said opening (242) through said plate member (240) in order to form an ink receiving cavity (250) thereunder, said heating resistor (209) being positioned beneath and in alignment with said ink receiving cavity (250), in order to impart heat thereto.

48/3,AB/9 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009098782
WPI Acc No: 1992-226215/199227
XRAM Acc No: C92-102269
XRPX Acc No: N92-171939
Thermal **ink-jet print-head** structure - uses conductive system for connecting driver **circuitry** and heating resistors, both formed on common **substrate**
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: FASEN D A; HESS U E
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5122812	A	19920616	US 91637387	A	19910103	199227	B
EP 493897	A2	19920708	EP 91311353	A	19911205	199228	
JP 4296565	A	19921020	JP 91358757	A	19911227	199248	
EP 493897	A3	19921014	EP 91311353	A	19911205	199340	
EP 493897	B1	19950614	EP 91311353	A	19911205	199528	
DE 69110441	E	19950720	DE 610441	A	19911205	199534	
			EP 91311353	A	19911205		

Priority Applications (No Type Date): US 91637387 A 19910103
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5122812	A		13	B41J-002/05	
EP 493897	A2	E	14	B41J-002/16	
Designated States (Regional): DE FR GB IT					
JP 4296565	A		8	B41J-002/16	
EP 493897	B1	E	22	B41J-002/16	
Designated States (Regional): DE FR GB IT					
DE 69110441	E			B41J-002/16	Based on patent EP 493897
EP 493897	A3			B41J-002/05	

Abstract (Basic): US 5122812 A
Structure comprises: a **substrate**; a drive **transistor**, pref. a **MOSFET**; a layer of metallic resistive material in direct contact with the **transistor** contact regions; a layer of metallic conductive material covering a portion of the resistance layer, the exposed portion acting as a resistive heater and the covered portion including the **transistor** contact regions; a portion of protective material positioned on the heating resistor; and a plate member with at least one opening secured to the protective material which has a via beneath the opening through to the resistive heater, forming an ink receiving cavity.
The resistive ayer is pref. a TaAl layer and the conductive layer is Al, Cu or Au. The protective portion comprises: an Si3N4 layer; an SiC layer; a Ta, W or Mo cavitation layer; and a plastic ink barrier layer to which the plate member is secured.
ADVANTAGE - **Printhead** is provided which operates efficiently and is readily mfd. in a min. number of steps.

Dwg.11/11

Abstract (Equivalent): EP 493897 B

Structure comprises a **substrate**; a drive **transistor**, pref. a **MOSFET**; a layer of metallic resistive material in direct contact with the **transistor** contact regions; a layer of metallic conductive material covering a portion of the resistive layer, the exposed portion acting as a resistive heater and the covered portion including the **transistor** contact regions; a portion of protective material positioned on the heating resistor; and a plate member with at least one opening secured to the protective material which has a via beneath the opening through to the resistive heater, forming an ink receiving cavity.

The resistive layer is pref. a TaAl layer and the conductive layer is Al, Cu or Au. The protective portion comprises an Si3N4 layer; an SiC layer; a Ta, W or Mo cavitation layer; and a plastic ink barrier layer to which the plate member is secured.

ADVANTAGE - **Printhead** is provided which operates efficiently and is readily mfd. in a min. number of steps.

(Dwg.11/11)

EP-493897 Structure comprises: a **substrate**; a drive **transistor**, pref. a **MOSFET**; a layer of metallic resistive material in direct contact with the **transistor** contact regions; a layer of metallic conductive material covering a portion of the resistance layer, the exposed portion acting as a resistive heater and the covered portion including the **transistor** contact regions; a portion of protective material positioned on the heating resistor; and a plate member with at least one opening secured to the protective material which has a via beneath the opening through to the resistive heater, forming an ink receiving cavity.

The resistive ayer is pref. a TaAl layer and the conductive layer is Al, Cu or Au. The protective portion comprises: an Si3N4 layer; an SiC layer; a Ta, W or Mo cavitation layer; and a plastic ink barrier layer to which the plate member is secured.

ADVANTAGE - **Printhead** is provided which operates efficiently and is readily mfd. in a min. number of steps.

EP-493897 A thermal **ink jet printhead** apparatus comprising a **substrate** (70); at least one drive **transistor** (74) formed on said **substrate** (70), said drive **transistor** (74) comprising a plurality of electrical contact regions (76, 78, 79) thereon; a layer (80) of electrically resistive material affixed to said **substrate** (70), said layer (80) of electrically resistive material being in direct physical contact with said electrical contact regions (76, 78, 79) of said drive **transistor** (74); a layer of conductive material affixed to a portion of said layer (80) of electrically resistive material in order to leave at least one uncovered section thereof, said uncovered section functioning as a heating resistor said layer (80) of electrically resistive material being covered with said layer of conductive material at said electrical contact regions (76, 78, 79) of said drive **transistor** (74); a portion of protective material positioned on said heating resistor; and a plate member having at least one opening therethrough, said plate member secured to said portion of protective material having at least one opening therethrough, said portion of protective material having a section thereof removed directly beneath said opening through said

48/3,AB/10 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06173625
INK-JET PRINTER WITH **PRINTHEAD** HAVING INTEGRAL **SUBSTRATE** HEATER DRIVER

PUB. NO.: 11-115173 [JP 11115173 A]
PUBLISHED: April 27, 1999 (19990427)
INVENTOR(s): ANDERSON FRANK EDWARD
EDWARDS MARK JOSEPH
GIBSON BRUCE DAVID
PARISH GEORGE KEITH
APPLICANT(s): LEXMARK INTERNATL INC
APPL. NO.: 10-229243 [JP 98229243]
FILED: July 09, 1998 (19980709)
PRIORITY: 891522 [US 891522], US (United States of America), July 11, 1997 (19970711)

ABSTRACT
PROBLEM TO BE SOLVED: To obtain a **printhead** which does not need an additional electric mutual connection for starting of a **substrate** heater, by setting a **substrate** heater driver and a decoder on the printing head integrally with the **printhead**.
SOLUTION: A-line driver 36 defines an electric **circuit** including a plurality of outputs EA1-EA5 respectively connected to pins EA1-EA5 of a **printhead** 10. The outputs EA1-EA5 are connected to second terminals of corresponding jet heaters of the **printhead** 10 via a decoder 24. The encoded outputs EA1-EA5 may be selectively energized to transmit coded enable signals to the decoder 24. The decoder then decodes the encoded signals and uses the decoded signals to actuate a **MOS transistor** 22 and/or a **transistor** 26 connected thereto.

57/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008270514
WPI Acc No: 1990-157515/199021
XRPX Acc No: N90-122435
Thermal **print head** with high density of heating elements - combines latched shift register print and power **MOSFET circuits** for heating elements on same **substrate**
Patent Assignee: CASIO COMPUTER CO LTD (CASK)
Inventor: OCHI T; WAKABAYASH T; WAKABAYASHI T
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 369347	A	19900523	EP 89120874	A	19891110	199021	B
JP 2137942	A	19900528	JP 88290287	A	19881118	199027	
US 5055859	A	19911008	US 89430885	A	19891102	199143	
KR 9310459	B1	19931025	KR 8914653	A	19891013	199439	
EP 369347	B1	19950524	EP 89120874	A	19891110	199525	
DE 68922823	E	19950629	DE 622823	A	19891110	199531	
			EP 89120874	A	19891110		

Priority Applications (No Type Date): JP 8976237 A 19890328; JP 88290287 A 19881118; JP 88287549 A 19881116
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 369347	A				
Designated States (Regional): DE FR GB					
EP 369347	B1	E	23	H01L-049/02	
Designated States (Regional): DE FR GB					
DE 68922823	E			H01L-049/02	Based on patent EP 369347
KR 9310459	B1			B41J-002/345	

Abstract (Basic): EP 369347 A

A print driver **circuit** element with sections for holding pint data (3) and for supplying current (4) is formed by direct doping of the head **substrate** (10) on a monocrystalline Si wafer. The resistive heating elements (14) based on polycrystalline Si are formed on a protuberance (12) on the **substrate** (10) and adjusted to a predetermined resistance value by impurity diffusion.

An overall SiO2-Si3N4 protective **insulating film** (15) projects outward where it extends over the protuberance (12) and ensures contact with the sheet to be printed. Current is conveyed to the heating elements (14) by thin-film conductors (24, 28) from external terminals (11).

ADVANTAGE - High productivity is achievable with heating and print driver **circuit** elements **integrated** on a common insulating **substrate**. Assembly is simplified and reliability is maintained even after prolonged use. (20pp Dwg.No.1/12)

Abstract (Equivalent): EP 369347 B

A thermal **print head** comprising: a single-crystal semiconductor **substrate** (10); a print driver **circuit** element (3, 4) consisting of predetermined regions of said

semiconductor **substrate** (10) including impurities; heating resistance elements (14, 50) on said semiconductor **substrate** (10); a thin film conductor (24, 28; 54) for wiring, said conductor (24, 28; 54) and an **insulating** protective **film** (15; 15') covering said print driver **circuit** element (3) and said heating resistance elements (14, 50); characterised in that said print driver **circuit** element (4), respectively formed of **MOS-FETs**; and a polycrystalline silicon layer (14) is formed on said semiconductor **substrate** (10) including regions forming gate **electrodes** (234) of said **MOS-FETs** and regions forming said heating resistance elements (14; 50).

Dwg.1/12

Abstract (Equivalent): US 5055859 A

The thermal print hed comprises a head **substrate**, formed of a single-crystal silicon wafer, and a print driver **circuit** element. The print driver **circuit** element, which is formed by doping the head **substrate** directly with an impurity, is composed of an **MOSFET**, A **FET** used to form the single-crystal silicon **substrate** has high electrical mobility, and serves to improve the operating speed of the thermal **print head**. Each heating resistance element, whose base material is polycrystalline silicon, is adjusted to a predetermined resistance value by being subjected to diffusion of an impurity. The resistance elements are formed on a protuberance which is formed on the head **substrate**. Thus, the portion of an **insulating** protective **film** which corresponds to the protuberance projects outward from the rest thereby ensuring contact with a printing sheet. An earthing diode or laminate structure is used for an earth line of each heating resistance elements so that the resistance element is situated close to a side edge portion of the head **substrate**. ADVANTAGE - Has heating resistance elements arranged with high density.

(18pp

57/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007203123
WPI Acc No: 1987-200132/198729
XRAM Acc No: C87-083713
XRPX Acc No: N87-149811
Thermal **ink jet print head** structure - combined with **MOS** driver **circuit** in multi-level IC structure
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: HESS U E
Number of Countries: 006 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 229673	A	19870722	EP 87100521	A	19870116	198729	B
US 4719477	A	19880112	US 86820754	A	19860117	198804	
CA 1275854	C	19901106				199050	
EP 229673	B1	19920708	EP 87100521	A	19870116	199228	
DE 3780177	G	19920813	DE 3780177	A	19870116	199234	
			EP 87100521	A	19870116		

Priority Applications (No Type Date): US 86820754 A 19860117
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 229673	A	E	9		
Designated States (Regional): DE FR GB IT					
US 4719477	A		8		
EP 229673	B1	E		B41J-002/16	
Designated States (Regional): DE FR GB IT					
DE 3780177	G			B41J-002/16	Based on patent EP 229673

Abstract (Basic): EP 229673 A
Mfr. of a **printhead** structure for a thermal **ink jet printhead** involves depositing, in succession on a **substrate** support member, a resistive heater layer material and a conductive trace pattern to define the lateral extent of heater resistors. The novelty is that the resistive material is polycrystalline silicon or a refractory and that the conductive patternis of a refractory metal deposited to provide a **path** for drive current to predefined areas in the resistive material.
An electronic device, specifically a thermal **ink jet printhead** structure, of the above design, is also claimed.
ADVANTAGE - The design provides improved resistance to ink penetration, corrosion and cavitation wear and combines **printhead** interconnect metallisation with **MOS** pulse drive **circuit** metallisation in a novel multilevel **MOS** IC structure.
0/2
Abstract (Equivalent): EP 229673 B
Mfr. of a **printhead** structure for a thermal **ink jet printhead** involves depositing, in succession on a **substrate** support member, a resistive heater layer material and a conductive trace pattern to define the lateral extent of heater

resistors. The novelty is that the resistive material is polycrystalline silicon or a refractory and that the conductive patternis of a refractory metal deposited to provide a **path** for drive current to predefined areas in the resistive material.

An electronic device, specifically a thermal **ink jet printhead** structure, of the above design, is also claimed.

ADVANTAGE - The design provides improved resistance to ink penetration, corrosion and cavitation wear and combines **printhead** interconnect metallisation with **MOS** pulse drive **circuit** metallisation in a novel multilevel **MOS** IC structure. (9pp Dwg.No.0/2)

Abstract (Equivalent): US 4719477 A

Thermal **ink jet print head** has a Si **substrate** (1) on which is a thermal **insulation layer** (2) of Si **dioxide**, a **layer** of Si nitride (3) being deposited on it. On this is a layer of resistive material (2), consisting of polycrystalline Si or refractory silicide selected from Ta, Ti, W, and Mo silicides, followed by a layer (5) of a chosen refractory metal from the gp. W, Ta, Ti, Mo, and a further thicker layer (6). After etching the conductive and resistive layers (4,5,6) in the required geometry, a layer of Si nitride (7) is deposited, then a layer of P-doped glass (8), SiO2, the structure being annealed to reflow the glass over resistor terminations. A layer (9) of phosphosilicate glass, P-doped, is applied and triple layer passivation (7,8,9) is dry etched to the refractory metal layer (6). Cavitation barrier (10) of Ta and final interconnect layer (11) of Al complete the structure.

ADVANTAGE - Refractory metal allows reflow of glass and sealing of resistor **electrode** terminations, Si nitride acting as oxidn. and moisture barriers, structure being compatible with **integrated circuit** processing. (8pp)f

60/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013167707
WPI Acc No: 2000-339580/200029
XRAM Acc No: C00-103042
XRPX Acc No: N00-254952
Inkjet printhead for **inkjet** printers has a series of nozzles for the ejection of ink, each nozzle having a rim formed by the deposition of a rim material layer over a sacrificial layer and subsequent planar removal of the rim layer
Patent Assignee: SILVERBROOK RES PTY LTD (SILV-N); SILVERBROOK K (SILV-I)
Inventor: SILVERBROOK K
Number of Countries: 091 Number of Patents: 012
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200023279	A1	20000427	WO 99AU894	A	19991015	200029	B
AU 200011391	A	20000508	AU 200011391	A	19991015	200037	
EP 1121249	A1	20010808	EP 99970634	A	19991015	200146	
			WO 99AU894	A	19991015		
US 6273544	B1	20010814	US 99425419	A	19991019	200148	
US 6299289	B1	20011009	US 99425416	A	19991019	200162	
US 6312114	B1	20011106	US 99425421	A	19991019	200170	
US 6309048	B1	20011030	US 99425418	A	19991019	200172	
US 20020024569	A1	20020228	US 99425191	A	19991019	200220	
			US 2001942604	A	20010831		

Priority Applications (No Type Date): AU 987023 A 19981109; AU 986534 A 19981016; AU 986535 A 19981016; AU 986536 A 19981016; AU 986537 A 19981016; AU 986538 A 19981016; AU 986539 A 19981016; AU 986540 A 19981016; AU 986541 A 19981016; AU 986542 A 19981016; AU 986543 A 19981016; AU 986544 A 19981016; AU 986545 A 19981016; AU 987022 A 19981109
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6273544	B1			B41J-002/01	
US 6299289	B1			B41J-002/04	
US 6312114	B1			B41J-002/175	
US 6309048	B1			B41J-002/04	

Abstract (Basic): WO 200023279 A1
Abstract (Basic):
NOVELTY - An **inkjet printhead** has a series of nozzles for the ejection of ink. Each nozzle has a rim formed by the deposition of a rim material layer (42) over a sacrificial layer (41) and subsequent planar removal of the rim layer to form the nozzle rim.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(A) A method of forming an **inkjet printhead** on a substrate, comprising:
(a) providing a first substrate where electrical drive **circuitry** made up of layers of conductive, semi-conductive and non-conductive materials is formed, for the control of **inkjet**

printhead; and

(b) forming on the substrate a nozzle chamber with ink ejection aperture in a wall and ink external thermal actuator to eject ink from the aperture, where portions of one of the substrate's layers are utilized as a sacrificial material layer in the formation of ink actuator. (B) A method of operation of a fluid ejection **printhead** within a predetermined thermal range so as to print an image, comprising:

(a) sensing the **printhead** temperature to determine if it is below a predetermined threshold;

(b) preheating the **printhead** is temperature is below the threshold;

(c) controlling the preheating such that thermal actuators are heated to an extent insufficient to eject fluid from the **printhead**; and

(d) utilizing the **printhead** to print the image.

(C) A fluid ejection device comprising an array of nozzles formed on a substrate and adapted to eject ink on demand using the ink actuators, a temperature sensor attached to substrate, and a temperature sensor unit.

(D) An ink supply arrangement for supplying ink to the printing arrangement of a portable printer, including an ink supply unit with a storage chamber for holding ink and a series of spaced apart baffles to reduce the acceleration of the ink within the unit as may be induced by movement of the printer while allowing for flows of ink to the printing arrangement in response to active demand.

(E) A power distribution arrangement for an elongate **inkjet printhead** with spaced voltage supply points, including two or more elongate low resistance power supply busbars, and tape automated bonded (TAB) film to connect selected supply points to the busbars.

(F) An ink supply unit for supplying a **printhead** containing an array of ink ejection nozzles, comprising baffles having a cavity and/or in the form of ink distribution manifold with a second cavity for the insertion of **printhead**.

(G) A method of interconnecting a **printhead** to an ink distribution manifold, comprising attaching the **printhead** to the manifold using a resilient adhesive to be elastically deformed with any deflections of the manifold.

(H) A **printhead** and ink distribution manifold assembly. (I) A method of improving the operational characteristics of the **printhead** comprising locating an end portion on the movable paddle, the portion moving towards the nozzle aperture upon activation of the liquid ejection paddle to eject the fluid.

(J) An **inkjet printhead** apparatus comprising nozzle chambers, ink supply channel interconnected with the chamber, paddle and an end portion interconnecting the paddle's portion.

USE - For **inkjet** printers.

ADVANTAGE - The **printhead** has high resolution which allows full photographic quality color images and high quality text. It allows high-speed operation, as no scanning is required. It is inexpensive and compact because as the nozzle density of the **printhead** is very high, the chip area per **print head** can be low, thus allowing multiple head designs. The **printhead**'s high resolution allows a fully digital operation using digital half toning which

eliminates color non-linearity. The **printhead** has small drop volume and accurate control of drop velocity. It allows fast drying and eliminates paper cockle. It has a wide temperature range and requires no special manufacturing equipment in moving from laboratory to production. It has high production capacity available, provides low factory setup cost, good light-fastness, good water-fastness, excellent color gamut, eliminates color bleed and has high nozzle count. No precision assembly is required because the **printhead** is made as a single monolithic **CMOS** chip. The **printhead** allows duplex printing at full print speed and is more efficient. It generates low pressure, requires low power, operates at low voltage and has low power consumption that a photographic **printhead** can operate from AA batteries. Manufacturing process is less complex and packaging is of low cost. The **printhead** has no thermal, fluidic or structural crosstalk, no cavitation or electromigration. It has reliable power connections and has no corrosion, electrolysis, fatigue, friction, crack propagation or rectified diffusion. It requires no electrical poling, eliminates saw street and is tuned for a wide variety of inks.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of a process on constructing an **ink jet** nozzle.

Sacrificial layer (41)

Rim material layer (42)

60/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008776965
WPI Acc No: 1991-280981/199138
Related WPI Acc No: 1991-352594
XRPX Acc No: N91-214777
Thermal ink drop-on-demand devices - is mounted on single chip with vertical integration of driver device
Patent Assignee: LEXMARK INT INC (LEXM-N); IBM CORP (IBMC)
Inventor: KACHMARIK R; LAMEY P
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5045870	A	19910903	US 90503353	A	19900402	199138	B
EP 452663	A	19911023	EP 91103578	A	19910308	199143	
EP 452663	B1	19940615	EP 91103578	A	19910308	199423	
DE 69102479	E	19940721	DE 602479	A	19910308	199429	
			EP 91103578	A	19910308		
JP 7068759	A	19950314	JP 9141217	A	19910213	199519	

Priority Applications (No Type Date): US 90503353 A 19900402
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 452663	A				
Designated States (Regional): DE FR GB					
EP 452663	B1	E	14	B41J-002/05	
Designated States (Regional): DE FR GB					
DE 69102479	E			B41J-002/05	Based on patent EP 452663
JP 7068759	A		10	B41J-002/05	

Abstract (Basic): US 5045870 A
This integrated **printhead** chip is made by first fabricating on the substrate the driver pulse **circuitry** through the last level of metallisation. Once complete, a low temp. CVD oxide is deposited and planarised. It is of sufficient thickness (3 to 4 microns) to insure a good thermal barrier between the pulse **circuitry** and the thermal **ink jet** devices.
After planarisation, the resistor material is deposited and patterned. Openings are then patterned to the inputs and outputs of the pulse driver **circuitry**. **Aluminium copper** metallurgy is deposited and patterned to connect the resistor to the pulse driver output and define the heater resistor areas. Inorganic and organic barrier layers are applied and pattnered to protect the resistor material and interconnecting metallurgy from the corrosive effects of the ink.
ADVANTAGE - Vertically **integrates** printer **MOS** driver **circuitry** with **ink jet** heater resistors on same chip.
Dwg.2B/3
Abstract (Equivalent): EP 452663 B
A method for fabricating a vertically integrated thermal **ink jet printhead** wherein at least a portion of a thermal

ink jet device is disposed over an **FET** pulse driver device (13) on a semiconductor substrate (11), said method comprising the steps of: providing said **FET** pulse driver device on a semiconductor substrate; depositing a thermal barrier layer (15) over said **FET** pulse driver device; planarising said thermal barrier layer; fabricating said thermal **ink jet** device on said planarised thermal barrier layer over said **FET** pulse driver device; and etching contact holes through said thermal barrier layer to allow electrical contact between said **FET** pulse driver device and said thermal **ink jet** device and between said **FET** pulse driver device and a **circuit** which couples said **integrated printhead** to a thermal **ink jet** printer.

60/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008644320
WPI Acc No: 1991-148350/199120
XRAM Acc No: C91-064144
XRPX Acc No: N91-113893
Ink jet print-head having electronic **circuitry** - ionically passivated with layers of **silicon dioxide, silicon, nitride,** and polyimide
Patent Assignee: XEROX CORP (XERO)
Inventor: ATKINSON D; BURKE C J; HARTMAN P J; HAWKINS W G; ROLL D O; ROLL D ; ATKINSON D M
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5010355	A	19910423	US 89456431	A	19891226	199120	B
EP 434946	A	19910703	EP 90121502	A	19901109	199127	
EP 434946	A3	19920102	EP 90121502	A	19901109	199320	
EP 434946	B1	19941019	EP 90121502	A	19901109	199440	
DE 69013480	E	19941124	DE 613480	A	19901109	199501	
			EP 90121502	A	19901109		

Priority Applications (No Type Date): US 89456431 A 19891226
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 434946	A				
	Designated States (Regional): DE FR GB				
EP 434946	B1	E	15	B41J-002/16	
	Designated States (Regional): DE FR GB				
DE 69013480	E			B41J-002/16	Based on patent EP 434946

Abstract (Basic): US 5010355 A

Ink jet printhead (10) has parallel ink flow channels, each terminating with an ink droplet emitting nozzle (27) at one end and communicating with an ink supplying reservoir at the other. A heating element (34) with a cavitational protective layer (17) is located in each channel a predetermined distance upstream from the nozzle and **MOS** electronic **circuitry** (48) is monolithically **integrated** within the **printhead** for applying electrical pulses to the heating elements to produce bubbles momentarily on the protective layer, each bubble causing an ink droplet to be expelled from a nozzle. The **MOS** electonic **circuitry** is ionically passivated through the deposition of a multi-layered, thin film, insulative coating consisting of a layer (16) of doped or undoped **silicon dioxide**, 200 A - 2 micron thick, directly over it and the heating elements, and a second layer (13) of plasma **silicon nitride**, 1000 A - 3 micron thick, over the first layer. The nitride layer and the **silicon dioxide** layer are dry etched from the heating elements and electrical contact pads to enable connection to electrical power, the etch sequence preventing the both the contact pads and heating element protective layers from being

attacked.

USE/ADVANTAGE - The **MOS circuitry** is concurrently protected from mobile ions in the ink by the multi-layered, ionic passivation while maintaining the cost effective fabrication of a **printhead** having heating elements with a cavitational protective layer to enhance life expectancy. (11pp Dwg.No.2/5)

Abstract (Equivalent): EP 434946 B

Ink jet printhead (10) has parallel ink flow channels, each terminating with an ink droplet emitting nozzle (27) at one end and communicating with an ink supplying reservoir at the other. A heating element (34) with a cavitational protective layer (17) is located in each channel a predetermined distance upstream from the nozzle and **MOS** electronic **circuitry** (48) is monolithically **integrated** within the **printhead** for applying electrical pulses to the heating elements to produce bubbles momentarily on the protective layer, each bubble causing an ink droplet to be expelled from a nozzle. The **MOS** electonic **circuitry** is ionically passivated through the deposition of a multi-layered, thin film, insulative coating consisting of a layer (16) of doped or undoped **silicon dioxide**, 200 A - 2 micron thick, directly over it and the heating elements, and a second layer (13) of plasma **silicon nitride**, 1000 A - 3 micron thick, over the first layer. The nitride layer and the **silicon dioxide** layer are dry etched from the heating elements and electrical contact pads to enable connection to electrical power, the etch sequence preventing the both the contact pads and heating element protective layers from being attacked.

USE/ADVANTAGE - The **MOS circuitry** is concurrently protected from mobile ions in the ink by the multi-layered, ionic passivation while maintaining the cost effective fabrication of a **printhead** having heating elements with a cavitational protective layer to enhance life expectancy. (11pp Dwg.No.2/5)

EP-434946 An **ink jet printhead** (10) having a plurality of parallel ink flow channels each of which terminate with an ink droplet emitting nozzle (27) at one end and communicate with an ink supplying reservoir at the other end, a heating element with a cavitational protective layer thereover being located in each channel a predetermined distance upstream from the nozzle (27), and **MOS** electronic **circuitry** monolithically **integrated** within the **printhead** for applying electrical pulses to the heating elements to produced bubbles momentarily on the protective layer of the heating element in response thereto, each of said bubbles expelling an ink droplet from the nozzles characterised in that ionic passivation of the **MOS** electronic **circuitry** through the deposition of a multi-layered, thin film insulative coating thereon consisting of a first layer of doped or undoped **silicon dioxide** directly over the **MOS** electronic **circuitry** and heating elements with protective layer having a thickness of 200 Angstrom to 2 micron followed by a second layer of plasma nitride over the first laye having a thickness of 1000 Angstrom to 3 micron, the **silicon nitride** being dry etched over the protective layer of the heating elements and electrical contact pads for external connection to electrical power to expose the first layer of silicon oxide, followed by etching of the silicon oxide to remove it from the protective layer

and contact pads (32,37) whereby the etch sequence prevents both contact pads (32,37) and the heating element protective layers from being attacked, and the **MOS circuitry** is concurrently protected from mobile ions in the ink by said multi-layered, ionic passivation, while maintaining the cost-effective fabrication of a **printhead** having heating elements with a cavitational protective layer to enhance their lifetime.

(Dwg.1/5

60/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008535982
WPI Acc No: 1991-040045/199106
XRPX Acc No: N93-174749
Combined reader and **print head** for copier and facsimile - has **MOS** photoelectric converter and scanner element in input and shift register, latch and thin film heater in output NoAbstract Dwg 2/3
Patent Assignee: CASIO COMPUTER CO LTD (CASK)
Inventor: OCHI T
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2306760	A	19901220	JP 89126707	A	19890522	199106	B
US 5227810	A	19930713	US 90508079	A	19900411	199329	

Priority Applications (No Type Date): JP 89126707 A 19890522; JP 89120395 A 19890516; JP 89124511 A 19890519
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5227810	A		15	H04N-001/028	

Abstract (Equivalent): US 5227810 A

The image reader and thermal recorder comprises a substrate, an image **circuit** section and a thermal display **circuit** section. The substrate is formed of either a monocrystalline silicon wafer or insulating material such as ceramics, glass or **quartz** having a polycrystalline silicon layer on the surface.

The image **circuit** section comprises photoelectric conversion cells and transfer **circuit** elements for transferring signals charged in each of photoelectric cells, which are integrally formed in and on the substrate. The display **circuit** section comprises a shift register for registering display data sensed by photoelectric cells, latch **circuit**, resistive heating elements including polycrystalline silicon layer and display driving elements, which are also integrally formed in and on the substrate.

ADVANTAGE - Is formed as integral unit on single substrate. (First major country equivalent to JP2306760)

(Dwg.1/7

60/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008530145
WPI Acc No: 1991-034229/199105
XRPX Acc No: N93-174749
Image input-output device for thermal printer - has thermal **print head** element and drive **circuit** on substrate on which **MOS** photoelectric converter is formed NoAbstract Dwg 1/2
Patent Assignee: CASIO COMPUTER CO LTD (CASK)
Inventor: OCHI T
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2305171	A	19901218	JP 89124511	A	19890519	199105	B
US 5227810	A	19930713	US 90508079	A	19900411	199329	

Priority Applications (No Type Date): JP 89124511 A 19890519; JP 89120395 A 19890516; JP 89126707 A 19890522
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5227810	A		15	H04N-001/028	

Abstract (Basic): JP 2305171 A
Dents (20) with which a mask member (19), having an annular aperture, is engaged are formed in the part contacting an island suspension lead (16) of the mask member (10).
USE/ADVANTAGE - Plating of an annular part to an IC lead frame having a bent part at a suspension lead is economically effected. (3pp Dwg.No.1,2,3,4,5/5)

Abstract (Equivalent): US 5227810 A
The image reader and thermal recorder comprises a substrate, an image **circuit** section and a thermal display **circuit** section. The substrate is formed of either a monocrystalline silicon wafer or insulating material such as ceramics, glass or **quartz** having a polycrystalline silicon layer on the surface.
The image **circuit** section comprises photoelectric conversion cells and transfer **circuit** elements for transferring signals charged in each of photoelectric cells, which are integrally formed in and on the substrate. The display **circuit** section comprises a shift register for registering display data sensed by photoelectric cells, latch **circuit**, resistive heating elements including polycrystalline silicon layer and display driving elements, which are also integrally formed in and on the substrate.
ADVANTAGE - Is formed as integral unit on single substrate. (First major country equivalent to JP2306760)
Dwg.1/7

60/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

002381662
WPI Acc No: 1980-J8130C/198041
Portable register with thermal printer - has facility for time data display on liq. crystal elements or by thermal printer
Patent Assignee: DAINI SEIKOSHA KK (DASE)
Inventor: KUROSAWA M; UCHIYAMA T
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 3010588	A	19801002				198041	B
GB 2045490	A	19801029				198044	
GB 2045490	B	19820902				198235	

Priority Applications (No Type Date): JP 7934075 A 19790323

Abstract (Basic): DE 3010588 A
A portable data register includes a thermal printer and a liquid crystal display. The unit is of use for athletics, medical and industrial applications, where it is required to record the start and end times. The compact housing (2) has a main on-off supply switch (5) and a liquid crystal display (3). A thermal printer (1) allows characters to be provided as print out.
The unit has a strip (2) **print head.** A separate switch (4) controls the activation of the printer. A **CMOS circuit** provides the timing function and is controlled by a **quartz** oscillator. A drive stage provides pulses for the printer stepping motor.

63/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008660016
WPI Acc No: 1991-164043/199122
XRPX Acc No: N91-125711
Printer operation with power supplied from rechargeable battery - features standby mode with reduced current compsn. and isolation of printer during active period of charger
Patent Assignee: SIEMENS AG (SIEI); EASTMAN KODAK CO (EAST)
Inventor: AL-KHATIB M; DREES F; EILER W; PEKRUHN W; PHAM N Q; ALKHATIB M; DREES F W; PHAM N
Number of Countries: 012 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
			WO 89DE699	A	19891102	
US 5449238	A	19950912	WO 89DE699	A	19891102	199542
			US 94855023	A	19940415	

Priority Applications (No Type Date): WO 89DE699 A 19891102
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9106430	A				
Designated States (National): JP US					
Designated States (Regional): AT BE CH DE FR GB IT LU NL SE					
US 5449238	A		7	B41J-029/38	Based on patent WO 9106430

Abstract (Basic): WO 9106430 A
A main switch (5) connects the printer to the battery (2) whose voltage is monitored by a flip-flop (11) driving a SIPMOS **FET** switch (12).
When the voltage falls below the reference level, a comparator (14) causes the control **circuit** (22) which governs the **print head** (23) to clock (36) the flip-flop (11) and open the **FET** switch (12) while the charger (3) is operative. This switch (12) is opened also after a predetermined max. time in the standby mode has elapsed.
ADVANTAGE - Max. number of printing operations can be performed without risk of deep discharge of battery. (17pp Dwg.No.1/2
Abstract (Equivalent): EP 500520 B
Process for the operation of a **recording device** (1) supplied by at least one rechargeable accumulator (2) with a charging device (3) which can be connected and disconnected, a control (22), a main switch (5) for startup and shutdown (Z1) of the **recording device** (1) and with at least one electrical switch (12) for separating the **recording device** (1) from the accumulator (2), whereby after being put into operation, the **recording device** (1) is moved into a waiting state (Z3) or into a state of being ready for recording (Z4) if the charging state of the accumulator (2)lies above a limiting value which is adequate for a recording procedure, after being put into operation, the **recording device** (1) is moved into the waiting state (Z3), in which the energy take-up of the control (22) - compared with the state (Z4) of

being ready for recording - is reduced, and the accumulator (2) is charged if the charging state of the accumulator (2) lies below the limiting value and the charging device (3) is connected, upon the occurrence of an activation signal the **recording device** (1) is moved from the waiting state (Z3) into the state (Z4) of being ready for recording if the charging state of the accumulator (2) lies above the limiting value, upon the occurrence of a deactivation signal the **recording device** (1) is moved from the state (Z4) of being ready for recording into the waiting state (Z3), and by means of the electrical switch (12) the **recording device** is moved into the electrically disconnected state (Z2) when the charging state of the accumulator lies below the limiting value and the charging device is disconnected.

Dwg.1/2

Abstract (Equivalent): US 5449238 A

The method involves placing the **recording device** into the operative state after start-up, if the state of the charge of the accumulator is above a limit. Placing the **recording device** into a stand-by state following start-up, if the state of charge of the accumulator is below the limit and the charger is connected.

This reduces the power consumption of the control relative to the operative state.

Charging the accumulator and placing the **recording device** into the operative state from the stand-by state when an activation signal occurs if the state of the charge of the accumulator is above the limit. Placing the **recording device** in the stand-by state from the operative state when a deactivation signal occurs. Placing the **recording device** into an electrically shut-off state via the electric switch when the state of charge of the accumulator is below the limit and the charger is shut off.

65/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012981332
WPI Acc No: 2000-153185/200014
XRPX Acc No: N00-114168
Bump connection quality judging method for IC chip package - involves determining conduction level of judging bump, based on which connection state of other bumps is estimated
Patent Assignee: OKI DATA SYSTEMS KK (OKID)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2000013013	A	20000114	JP 98172726	A	1998061	200014	B

Priority Applications (No Type Date): JP 98172726 A 19980619
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2000013013	A		7	H05K-003/34	

Abstract (Basic): JP 2000013013 A
NOVELTY - A judging bump is provided on the surface of a circuit at a height less than that of connecting bumps (31). The quality of conduction of the judging bump is found, based on which quality of connection of the bump-row is judged. DETAILED DESCRIPTION - A space confirmation pad (22) is formed at both ends of connecting pads (21), which is formed on the surface of an LED array (2). The LED array is connected to the IC chip (1).
USE - For evaluating bump connection of IC chip package used in LED driver of **print head** in electrophotographic printer.
ADVANTAGE - Enables easy detection of partially connected bumps and thereby defective connection is avoided. DESCRIPTION OF DRAWING(S) - The figure shows the front elevation of bump connection quality judging method. (1) IC chip; (2) LED array; (21) Connecting pad; (22) Space confirmation pad; (31) Connecting bump.

65/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011634545
WPI Acc No: 1998-051673/199805
XRPX Acc No: N98-041062
Calibrating LED **print head** - using ageing characteristics of LEDs by ageing all LEDs into linear ageing region measuring light output of each and differentially ageing for different lengths of time
Patent Assignee: EASTMAN KODAK CO (EAST)
Inventor: FLEMING P J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5699103	A	19971216	US 94360156	A	19941220	199805	B

Priority Applications (No Type Date): US 94360156 A 19941220
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5699103	A		10	B41J-002/45	

Abstract (Basic): US 5699103 A

The **printhead** is calibrated to have reduced non-uniformities in the light outputs between LEDs on the **printhead**. The calibration involves burning-in all the LEDs until an aging characteristic of the LEDs is in a linear range of an aging curve. The light intensity emitted by each LED after the burning-in is measured. A target value is established for additional burning-in of LEDs having measured light intensities above a minimum measured light intensity. They are differentially aged by additional burning-in towards the target value.

The target value is a specified maximum average light level for the **printhead**. The minimum measured light intensity is greater than a specified maximum average light level for the **printhead**. Alternatively the target value is the lesser of a specified maximum average light level of the **printhead** and

MIN. multiply (1+a uniformity specification factor). The uniformity specification factor is a range of intensities that all recording elements on one **printhead** are required to be within. MIN. is the minimum measured light intensity.

USE - For gray scale imaging, for binary **printheads**, photosensitive media exposure.

ADVANTAGE - Achieves uniform **print head** even without correction data input.

68/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014605392
WPI Acc No: 2002-426096/200245
XRAM Acc No: C02-120728
XRPX Acc No: N02-335054
Compensating micro-machined electromechanical sensor device comprises forming oxide film with coefficient of thermal expansion different from that of substrate
Patent Assignee: DWYER P W (DWYE-I); HONEYWELL INT INC (HONE)
Inventor: DWYER P W; DWYER P
Number of Countries: 020 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200228766	A2	20020411	WO 2001US29996	A	20010924	200245	B
US 20020068370	A1	20020606	US 2000237954	P	20001003	200245	
			US 2001963142	A	20010924		

Priority Applications (No Type Date): US 2000237954 P 20001003; US 2001963142 A 20010924
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200228766	A2	E	23	B81C-005/00	
	Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR				
US 20020068370	A1			H01L-021/66	Provisional application US 2000237954

Abstract (Basic): WO 200228766 A2
Abstract (Basic):
NOVELTY - A micro-machined electromechanical sensor (MEMS) device is compensated by making the device in a substrate (211) having a first coefficient of **thermal** expansion; forming an **oxide** film (228) with a second coefficient of thermal expansion, on device surface area(s); and removing a portion of the oxide film from the device surface area(s).
USE - For compensating MEMS devices (claimed) e.g. accelerometer and rate sensors.
ADVANTAGE - The method provides a delicate adjustment of feature orientation in completed and operational MEMS devices with or without silicon cover plates. It allows trimming of modulation, bias, and other dynamic behaviors of the device after initial formation and installation within the device packaging.
DESCRIPTION OF DRAWING(S) - The drawing shows a MEMS device.
Substrate (211)
Frame (218)
Proof mass (220)
Flexures (222)
Oxide film (228)

68/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009057682
WPI Acc No: 1992-185064/199223
XRAM Acc No: C92-084708
XRPX Acc No: N92-139702
Analysing metal impurities in semiconductor substrate surface oxide - by measuring amt. of oxide charge resulting from impurities and obtaining correlation with amt. of metal impurities
Patent Assignee: SEIKO EPSON CORP (SHIH)
Inventor: KATO J
Number of Countries: 009 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 488149	A2	19920603	EP 91120154	A	19911126	199223	B
JP 5041433	A	19930219	JP 91309206	A	19911125	199312	
EP 488149	A3	19930317	EP 91120154	A	19911126	199350	
US 5298860	A	19940329	US 91796823	A	19911125	199412	
EP 488149	B1	19960508	EP 91120154	A	19911126	199623	
DE 69119365	E	19960613	DE 619365	A	19911126	199629	
			EP 91120154	A	19911126		
TW 312745	A	19970811	TW 91109236	A	19911125	199746	
SG 45200	A1	19980116	SG 961226	A	19911126	199811	
KR 163596	B1	19990501	KR 9121393	A	19911126	200051	

Priority Applications (No Type Date): JP 90321763 A 19901126
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 488149	A2	E	13	G01N-033/20	
Designated States (Regional): DE FR GB NL					
JP 5041433	A			H01L-021/66	
EP 488149	A3			G01N-033/20	
US 5298860	A		11	G01R-031/26	
EP 488149	B1	E	15	G01N-033/20	
Designated States (Regional): DE FR GB NL					
DE 69119365	E			G01N-033/20	Based on patent EP 488149
TW 312745	A			G01N-027/60	
SG 45200	A1			G01N-033/20	
KR 163596	B1			G01N-027/60	

Abstract (Basic): EP 488149 A

Metal impurities are analysed by: measuring an amt. of oxide charge resulting from metal impurities in the oxide film; obtaining a correlation between the charge and the amt. of metal impurities; and measuring the amt. of impurities based on the correlation and the amt. of oxide charge of the film.

The impurities are pref. Fe and/or **Al**. The oxide film is pref. a native **oxide** or **thermal oxide** film. The amt. of oxide charge resulting from the metal impurities is measured by obtaining a CV relation between a dc bias voltage V to the substrate and a depletion layer capacitance C by measuring a surface

photoelectric voltage generated by LED intermittent light. Alternatively, the amt. is measured by dissolving the film in clean HF and obtg. an atomic absorption spectrum.

USE/ADVANTAGE - Method is simple and low cost, does not need a vacuum and permits detection sensitivity of about 10 power 11 atoms/sq.cm.

Dwg.5/6

Abstract (Equivalent): EP 488149 B

A method of analysing metal impurities including at least one of iron and **aluminium**, in a surface oxide film formed on a semiconductor substrate, comprising: (a) measuring the quantity of oxide charge resulting from metal impurities existing in the surface oxide film; and (b) determining the quantity of metal impurities in the surface oxide film from the quantity of oxide charge measured in step (a) and a pre-established correlation between the quantity of oxide charge and the quantity of the metal impurities.

(Dwg.0/6

Abstract (Equivalent): US 5298860 A

Analysing metal impurities in an oxide film formed on a semiconductor substrate surface involves applying a DC bias voltage to the substrate and LED intermittent light to the oxide film in proportion to the width of a semiconductor depletion layer while varying the applied voltage. The relationship between voltage and depletion capacitance is determined from generated photoelectric voltage to measure Fe and/or **Al**.

ADVANTAGE - Method does not require a vacuum, detection sensitivity of 10'' atoms/cm2.

68/3,AB/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

00634571

METHOD OF TESTING SEMICONDUCTOR UNIT

PUB. NO.: 55-122171 [JP 55122171 A]
PUBLISHED: September 19, 1980 (19800919)
INVENTOR(s): IIZUKA TSUNEO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 54-029700 [JP 7929700]
FILED: March 14, 1979 (19790314)
JOURNAL: Section: P, Section No. 40, Vol. 04, No. 180, Pg. 22, December 12, 1980 (19801212)

ABSTRACT

PURPOSE: To avoid the adverse effect of irradiated light in measurement, by coating an **Al** film except on the electrode terminal face of a semiconductor unit produced on the surface of a semiconductor substrate by a photoresist method, and thereafter bringing a measuring probe into contact with the electrode terminal.

CONSTITUTION: A **phosphosilicate glass** film 7 is produced except on one electrode terminal 2 of a semiconductor unit 1 manufactured on a semiconductor substrate of a tested body. A photoresist film 8 is selectively provided on the film 7. An **Al** film 9 is produced on the entire surface of the film 8. The photoresist film 8 is thereafter removed by a lifting-off method. At the same time, the **Al** layer on the film 8 is also removed. As a result, the surface of the electrode terminal 2 is exposed. A second photoresist layer 10 having an opening on the surface of the electrode terminal is produced. The semiconductor unit is thus treated. A measuring probe 4 is brought into contact with the electrode terminal 2 to test the electric properties of the unit 1.

73/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012281495
WPI Acc No: 1999-087601/199908
Related WPI Acc No: 1995-112114; 1995-134754
XRPX Acc No: N99-063983
Probe unit for IC chip inspection - includes probe card which is arranged contacting **electrode** pads of target, is pressed due to pressure of **fluid** supplied from supply **path**
Patent Assignee: TOKYO ELECTRON LTD (TKEL)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
JP 10321686	A	19981204	JP 93201096	A	19930720	199908 B
			JP 98134652	A	19930720	

Priority Applications (No Type Date): JP 93201096 A 19930720; JP 98134652 A 19930720
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 10321686	A		10	H01L-021/66	Div ex application JP 93201096

Abstract (Basic): JP 10321686 A

The unit includes a container (2) having a stand (3) on which a target (**W**) to be inspected is mounted. Probe cards (40,41) are arranged contacting the **electrode** pads of the target. An external connector and the probe card contacts are connected, electrically.

Fluid is supplied to the probe card, from a supply **path** (6). The probe card is pressed on the target, due to the pressure of the supplied **fluid**. The target is examined by performing temperature control using a controller (32) provided in the container.

ADVANTAGE - Simplifies pressure adjustment process. Enables performing stable electric measurement. Enables performing highly precise alignment.

Dwg.1/7

73/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010210860
WPI Acc No: 1995-112114/199515
Related WPI Acc No: 1995-134754; 1999-087601
XRPX Acc No: N95-088243
Probe appts. for semiconductor wafer probe test, measuring electrical characteristics of IC chips on wafers - involves supply of **fluid** into damper chamber positions above probe card and pressing such that bumps in card contact wafer and receptacle **electrode**
Patent Assignee: TOKYO ELECTRON LTD (TKEL); TOKYO ELECTRON YAMANASHI LTD (TKEL)
Inventor: SANO K
Number of Countries: 003 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7037945	A	19950207	JP 93201096	A	19930720	199515	B
US 5550482	A	19960827	US 94274862	A	19940714	199640	
US 6072325	A	20000606	US 94274862	A	19940714	200033	

Priority Applications (No Type Date): JP 93201096 A 19930720; JP 93225210 A 19930818
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7037945	A		7	H01L-021/66	
US 5550482	A		15	G01R-001/073	
US 6072325	A			G01R-001/073	Div ex application US 94274862 Div ex patent US 5550482

Abstract (Basic): JP 7037945 A
The probe apparatus is formed by a receptacle (2) having a cover (21) and a base (22). A probe card (40) having two bumps (41, 42) is fixed to the cover. A wafer position stand (3) which supports the wafer (**W**) is fixed to the base. The base above the probe card forms a damper chamber (S1). A **fluid** is supplied to the chamber through a **fluid** supply **path** (6) and the probe card is pressed down so that the first bump contacts the wafer. The second bump (42) of the probe card is connected with an **electrode** (5) provided at the peripheral part of the receptacle.
USE/ADVANTAGE - Performs stable electric character measurement. Avoids influence of external electric noise. Remains unaffected by external temp.
Dwg.1/7
Abstract (Equivalent): US 5550482 A
A probe device, comprising:
a mounting stand for holding thereon an object to be tested, the object having **electrode** pads such that, when the object to be tested is held on said mounting stand, the **electrode** pads of the object to be tested face away from said mounting stand;
a probe card provided facing said mounting stand and therefore the **electrode** pads of an object to be tested held on said mounting stand, the probe card having contactors for contacting the **electrode** pads of an object to be tested held on said mounting

stand;

a test head for performing electrical measurements of an object to be tested held on said mounting stand;

connection means for electrically connecting said contactors of said probe card to said test head;

moving means for moving said probe card relative to said mounting stand such that, when an object to be tested is held on said mounting stand, said contactors are brought into contact with the **electrode** pads of the object to be tested, thereby causing the **electrode** pads to be electrically connected to said test head through the contactors and said connection means;

a vessel having an interior accommodating said mounting stand and said probe card in a sealed state, said vessel including

a first portion supporting said mounting stand; and

a second portion supporting said probe card, the second portion being relatively movable to and away from said first portion to hermetically close said vessel and to open the vessel so as to allow an object to be tested to be conveyed onto and away from said mounting stand;

a positioning unit for advancing into and out of a space between said mounting stand and said probe card when said first portion and said second portion are separated to open said vessel; and

an optical system provided on said positioning unit for transmitting an image of at least one **electrode** pad of an object to be tested held on said mounting stand, and for transmitting an image of at least one of said contactors of said probe card.

(Dwg.3/10

73/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008105715
WPI Acc No: 1989-370826/198950
Related WPI Acc No: 1991-267408; 1993-273041; 1993-352046; 1994-151601; 1995-328672; 1997-052499
XRAM Acc No: C89-164233
XRPX Acc No: N89-282235
Testing of **integrated circuit** at logic unit level - gives enhanced process yields by testing prior to interconnect metallisation
Patent Assignee: LEEDY G J (LEED-I); REEDY G J (REED-I); ELM TECHNOLOGY CORP (ELMT-N)
Inventor: LEEDY G J
Number of Countries: 015 Number of Patents: 013
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 8911659	A	19891130	WO 89US2088	A	19890515	198950	B
US 4924589	A	19900515	US 88194596	A	19880516	199024	
US 4994735	A	19910219	US 89436278	A	19891114	199110	
BR 8907190	A	19910305				199114	

Priority Applications (No Type Date): US 88194596 A 19880516; US 89436278 A 19891114; US 89436395 A 19891114; US 89436396 A 19891114; US 2001775598 A 20010205
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020045297	A1			H01L-021/00	Cont of application US 9827959

Abstract (Basic): WO 8911659 A

A method is provided for testing each transistor or logic unit on an **integrated circuit** wafer (1) prior to interconnect metallisation. The testing is carried out using a novel specially fabricated flexible tester surface (10) made of several layers of flexible **silicon dioxide**, each layer contg. vias and conductive traces leading to thousands of microscopic metal probe points (15) on one side of the test surface. **Fluid** pressure is used to ensure good electrical contact between these probe points (15) and the contacts (2) on the wafer (1) under test, and the tester surface traces are connected by a multiplexer to a conventional tester signal processor. Using CAD techniques, the transistor or logic unit placement net list is revised to substitute redundant defect-free logic units for defective ones, and then the interconnect metallisation is laid down under CAD control.

USE/ADVANTAGE - The method permits elimination of defects at the device level to give major increases in process yields, typically to about 90% regardless of die size, and also permits successful fabrication of very large die compared with conventional methods.

Dwg.6/6

Abstract (Equivalent): US 5034685 A

Test device comprises (a) support for wafer having **integrated circuit** units including electrical devices and **circuitry**

with contact points; (b) flexible tester surface with thickness up to 15 microns, having probe points corresp. to wafer contact points; (c) means for electrically connecting probe points and contact points; and (d) means to supply programmable input-output diagnostic signals to tester surface.

Pref. flexible material comprises thin sheet of low stress **silicon dioxide**.

USE/ADVANTAGE - To test logic units of **integrated circuit** formed on semiconductor wafer. Process yield is vastly improved, by as much as 90% compared to conventional testing. (13pp)

US 5020219 A

For resting **integrated circuits**, in which gate array transitors are arrayed on a wafer surface (1) and the active regions of each transistor are provided with contact points (2-1, 2-2) in columns and rows, a flexible tester surface (10) is used, including a series of tester contact points (15-1,15-02) and a complete wiring interconnection. Wafer and tester surface are positioned on a support (26) and a **fluid** well (38) is used to exert uniform pressure over the surface. Tester surface is mounted on a support ring (36).

ADVANTAGE - Prodn. yields are improved by testing at the logic unit level.

Dwg.5

US 4994735 A

A tester surface for **integrated circuits** has at least one flexible surface of silicon based material with a thickness not exceeding 15 microns on which multiple conductive vias are formed. A thin patterned film of metal deposited on the flexible material forms conductive traces and contact points for linking with the contacts on the **circuit** under test.

ADVANTAGE - By allowing 'fine-grain testing' of the individual **circuit** elements the reject level in the final **integrated circuit** device is substantially reduced.

US 4924589 A

An IC is mfd. by (a) simultaneously testing electrically isolated individual logic units prior to interconnection by contacting a flexible tester surface, comprising an SiO2 below 15 microns thick, with the units by **fluid** pressure exerted on the tester surface, (b) revising a net placement list of the 1C by CAD means to include only units that have passed the test, (c) interconnecting the units by a thin conductive film, and (d) electron beam patterning.

Pref. temporary interconnections are formed prior to testing, comprising a conductive layer and a dielectric layer. The tester surface has probe points 2-4 microns in dia. The tester pref. has a piezoelectric pressure cell behind the tester surface. The testing involves applying a voltage to the cell to effect contact with the logic units.

ADVANTAGE - Improved test procedure, increasing prodn.yields, compared to conventional testing at the functional IC level. Defects can be eliminated at device level. Successful mfr. of very large ICs compared to current technology.

73/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003918674
WPI Acc No: 1984-064218/198411
Related WPI Acc No: 1987-265191; 1987-265192
XRPX Acc No: N84-048585

Electronic test head positioner for test systems - offers six degrees of freedom and provides weightless condition to test head during docking and undocking with device handler

Patent Assignee: INTEST CORP (INTE-N); TEST CORP (TEST-N)
Inventor: SMITH N R
Number of Countries: 016 Number of Patents: 015
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 102217	A	19840307	EP 83304739	A	19830816	198411	B
JP 59060206	A	19840406	JP 83154237	A	19830825	198420	
US 4527942	A	19850709	US 82411311	A	19820825	198530	
US 4588346	A	19860513	US 83522635	A	19830811	198622	

Priority Applications (No Type Date): US 83522635 A 19830811; US 82411311 A 19820825; US 82UU11311 U 19820825; US 8722287 A 19870305; US 88265591 A 19881101; US 90501962 A 19900329; US 91744644 A 19910808
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5149029	A		17	A47G-029/00	CIP of application US 82411311
					Div ex application US 83522635
					Div ex application US 85753684
					Div ex application US 8722287

Abstract (Basic): EP 102217 A

An H-shaped beam forms the vertical column which is supported by the base assembly with base plate and outwardly extending legs. The test head is supported and manipulated in its docking by a positioner arm assembly moving vertically on the main shaft and counterbalanced by the counterweight assembly adjusted precisely to the weight of the positioner arm assembly plus the test head so that they function in a weightless state.

The counterweight **carriage** has vertically extending **carriage** shafts attached to the side walls of the main column section. The main arm assembly includes an upper bearing mount and lower bearing mount carried on a common block. The vertical and rotational movements of the arm assembly may be temporarily locked in any position.

73/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003102305
WPI Acc No: 1981-L2354D/198144
Semiconductor test unit for laboratories - has cross-table and circular slotted probe disc with monitor socket holder
Patent Assignee: STAUDTE B (STAU-I)
Inventor: STAUDTE B
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
DD 149965	A	19810805				198144 B
DD 149965	B	19830511				198336

Priority Applications (No Type Date): DD 220107 A 19800401
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DD 149965	A		10		

Abstract (Basic): DD 149965 A

A laboratory test unit for semiconductor components reduces testing time, technical and economical costs of testing, and servicing costs compared to conventional devices. It has a reduced trouble rate and is more convenient for servicing. Twenty four pole hybrid **circuits** can be tested using a single adjustment.

A cross-table with three linear and one rotational adjustments is placed in a vertically adjustable guide bush which can turn **w** .r.t. a frame. The probe system contains a probe carrying disc (19) attached to a **carriage** sliding vertically on the frame. The probes are placed in radial slots (20) so as to be linearly and rotationally adjustable. Monitor sockets for the probes are arranged on a circle and above the probes on a carrier screwed to the disc.

2

73/3,AB/6 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06038586
BURN-IN DEVICE

PUB. NO.: 10-321686 [JP 10321686 A]
PUBLISHED: December 04, 1998 (19981204)
INVENTOR(s): SANO KUNIO
APPLICANT(s): TOKYO ELECTRON LTD [367410] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 10-134652 [JP 98134652]
FILED: April 28, 1998 (19980428)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a burn-in device that can stably measure electrical characteristics regardless of ambient temperature.

SOLUTION: A container 2 that is constituted so that it can be divided into a cover part 21 where a probe card 40 is fixed integrally and a base part where a wafer placement stand 3 is fixed is used, and a wafer **W** and a flexible probe card 40 are closed into the container 2 while they oppose each other. The upper space of the probe card 40 is a damper room, and a **fluid** is injected into it and, for example, a collective contact type bump 41 of the probe card 40 is pressed to the side of the wafer **W** due to the pressure. A bump 42 at the periphery edge part of the probe card 40 and an **electrode** 5 of the peripheral edge of the container 2 are connected before being connected to a test head side.

73/3,AB/7 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05098945
TEST HEAD FOR IC TESTER

PUB. NO.: 08-054445 [JP 8054445 A]
PUBLISHED: February 27, 1996 (19960227)
INVENTOR(s): SHIMABARA NORIO
TSUKAHARA AKIO
GOI NORIYUKI
MOTOHASHI HIROAKI
APPLICANT(s): YOKOGAWA ELECTRIC CORP [000650] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-190345 [JP 94190345]
FILED: August 12, 1994 (19940812)

ABSTRACT

PURPOSE: To improve the mounting efficiency by radially arranging printed boards mounting electronic components on both sides, and providing a cooling plate for transferring the heat generated from the components to **fluid** to cool them.

CONSTITUTION: Printed boards 1, 3 are radially provided. The boards 1 of 32 pieces, for example, mount pin electronic **circuits** and timing generators, and the boards 2, 3 of 16 pieces mount DC/DC converters, etc. Cooling plates 4, 5 of 16 are formed, for example, out of an aluminum alloy, and mount the component mounting surfaces of the boards 1-3 on the both sides with screws, and have **copper** channel tubes therein to transfer the heat generated from the components to **fluid** to cool them. A manifold 6 receives cooling water from a heat exchanger, and distributes to supply it to the plates 4, 5. Thus, the board 1-3 are mounted on both the surface of the plates 4, 5 to cool the components, and hence the mounting efficiency is high and cooling capacity can be efficiently utilized.

73/3,AB/8 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

02350776
SEMICONDUCTOR ELEMENT EVALUATING DEVICE

PUB. NO.: 62-267676 [JP 62267676 A]
PUBLISHED: November 20, 1987 (19871120)
INVENTOR(s): USUI TOSHIO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-110833 [JP 86110833]
FILED: May 16, 1986 (19860516)
JOURNAL: Section: P, Section No. 698, Vol. 12, No. 147, Pg. 161, May 07, 1988 (19880507)

ABSTRACT

PURPOSE: To exactly execute a life test in a short period by taking sufficiently an earth of a high frequency, and reducing a heat conduction.

CONSTITUTION: As for a thin film 17, for instance, **Au** plating whose thickness is 50.mu.m is a **copper** foil, it is brazed to the back (high frequency earth part) of an input/output **circuit** substrate 13, and on its surface, a matching **circuit** 19 is formed. A high frequency loss (by an inductance component generated by the thin film 17) can be disregarded, and also, as for a heat block 15 which has contained a **cartridge** heater 22, a thermal isolation is obtained enough by packing its periphery with asbestos 23 by a holding plate 24 of stainless steel. Therefore, a difference between a package temperature of a device and a temperature of the input/output **circuit** substrate part can be obtained.

79/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010274827
WPI Acc No: 1995-176082/199523
XRPX Acc No: N95-138145
Hot carrier deterioration simulation method for **MOS** type **transistor** - by simulating hot carrier deterioration stress based on which rate of change of drain current with life time is determined by reserve experiment
Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ); MITSUBISHI DENKI KK (MITQ)
Inventor: SHIMIZU S; TANIZAWA M
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7099302	A	19950411	JP 93241161	A	19930928	199523	B
US 5508632	A	19960416	US 94262112	A	19940617	199621	
KR 146641	B1	19981102	KR 9424350	A	19940927	200028	

Priority Applications (No Type Date): JP 93241161 A 19930928
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7099302	A		15	H01L-029/00	
US 5508632	A		21	G01R-031/26	
KR 146641	B1			H01L-021/336	

Abstract (Basic): JP 7099302 A
The simulation method relates to N type **MOS transistor**, simulates data based on the following formulas; FN(t) = (**W**-B)-n, ISUBmn, id(1-m)n and tn, id/id = (id/id)f where FN (t) expresses the amount of hot carriers stress to time. `**W**' is the gate width of the **transistor**,`B' is the factor depending on the manufacturing `ISUB' is a **substrate** current, `id' is the drain current, `m' shows the index considered with reference to impact ionisation by hot carrier. `(id/id)f' shows the rate of change of drain current at the time of life time of **transistor** to previous drain current id. `n = g(VG)' depends on stress conditions rather than constant gate voltage (VG). The above relations are determined by reserve experiment.
ADVANTAGE - Simulates both by ac, dc current to provide accurate result.
Dwg.0/0
Abstract (Equivalent): US 5508632 A
A method of analyzing an **integrated circuit** of a semiconductor device comprising a plurality of components including an **N-MOS transistor**, which method comprises:
operating said semiconductor device;
predicting deterioration of the **N-MOS transistor** by simulating hot carrier deterioration; and
taking corrective action in response to simulating hot carrier deterioration by isolating areas of the **integrated circuit** susceptible to hot carrier degradation effects; wherein said simulating hot carrier deterioration of an **N-MOS transistor**

comprises formulas (6) and (7):

FN(t)=(**W**.B)-n.ISUBmn.ID(1-m)n.tn(6)

deltaID/ID=(deltaID/ID)f.FN(t)(7)

where FN(t) represents a quantity of a hot carrier stress applied until a time t, **W** represents a width of a gate of said **transistor**, B represents a coefficient depending on a manufacturing condition of said **transistor**, ISUB represents a **substrate** current, ID represents a drain current, m represents an index which is deemed to be correlated to impact ionization and generation of interface energy levels, and (deltaID/ID) represents a rate of a variation deltaID of said drain current at the time of expiration of a lifetime of said **transistor** to an initial value of said drain current ID, wherein

n is not a constant but is expressed as a function n=g(VG, VD) of a gate voltage VG and a drain voltage VD which are applied at the time of said hot carrier stress, and said function is determined by a preliminary experiment.

79/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008000639
WPI Acc No: 1989-265751/198937
XRPX Acc No: N89-202637
Current measuring **circuit** for **integrated circuit** - uses operational amplifier and **MOS transistor** to provide voltage directly proportional to current flow
Patent Assignee: SGS THOMSON MICROELTRN SA (SGSA); SGS-THOMSON MICROEL (SGSA)
Inventor: NADD B
Number of Countries: 007 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 332547	A	19890913	EP 89420083	A	19890307	198937	B
FR 2628217	A	19890908				198943	
JP 2010269	A	19900116	JP 8952202	A	19890306	199008	
US 4910455	A	19900320	US 89318869	A	19890306	199017	
EP 332547	B1	19930203	EP 89420083	A	19890307	199305	
DE 68904664	E	19930318	DE 604664	A	19890307	199312	
			EP 89420083	A	19890307		

Priority Applications (No Type Date): FR 883239 A 19880307
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 332547	A	F	7		
Designated States (Regional): DE FR GB IT NL					
EP 332547	B1	F	7	G01R-019/00	
Designated States (Regional): DE FR GB IT NL					
DE 68904664	E			G01R-019/00	Based on patent EP 332547

Abstract (Basic): EP 332547 A

The current measuring **circuit** includes an operational amplifier (22) whose inverting input is connected to earth via a first resistance (23) and second resistance (21) in series with it. The junction between these two resistances receives the current (InL) to be measured. The output of the operational amplifier is connected by an invertor (26) to an **MOS transistor** (27).

The bias voltage of the operational amplifier and the characteristics of the invertor are chosen so that the **MOS transistor** becomes biased at its threshold in the absence of current to be measured.

USE/ADVANTAGE - **Circuit** measures current in IC, providing output voltage (Vs) which is related to current by linear relationship independent of temp.

Abstract (Equivalent): EP 332547 B

A current measuring **circuit** for an **integrated circuit**, characterised in this that it comprises an operational amplifier (22) the inverting input terminal of which is grounded through a first resistor (23) having a value R(B) and a second resistor (21) having a value R(2), the junction of said two resistors receiving

the current (I(NL)) to be measured, the non-inverting input which is biased by a dividing bridge comprising a third resistor (24) having a value R(A) and a fourth resistor (25) having a value R(B) connected between a supply voltage and the ground, the output of which is connected to the input of an inverter (26), a **MOS transistor** (27) the gate of which is connected to the inverter output, the drain of which is connected to the supply voltage through a fifth resistor (29) having a value R1 and to the first input of the operational amplifier through a sixth resistor (30) having a value R(A), the source of which is grounded through a measurement resistor having a value Rs, the second and fifth resistors having low values w.r.t. the first, third, fourth and sixth resistors, the biasing voltage of the operational amplifier and the characteristics of the inverter being chosen so that the **MOS transistor** is biased at its threshold in the absence of a current to be measured, whereby the output voltage is correlated with the current to be measured by the linear relation Vs = ((1-K)/K)(R(2)/R(1))(I(NL))/Rs) where K = R(B)/(R(A)+R(B)). (Dwg.3/4)

Abstract (Equivalent): US 4910455 A

The **MOS** IC current measuring **circuit** comprises an operational amplifier (22), the non-inverting input terminal of which is grounded through a first resistor (23) having a value RB and a second resistor (21) having a value R2. The junction of those two resistors receives the current (INL) to be measured. The output of the amplifier is connected by an inverter (26) to a **MOS transistor** (27).

The biasing voltage of the operational amplifier and the characteristics of the inverter are chosen so that the **MOS transistor** is biased at its threshold in the absence of a current to be measured, thus the output voltage VS is correlated with the current to be measured by a linear relation independent of the temperature.

ADVANTAGE - Obtains measuring voltage independent of variations of temp. or other parameter of IC contg. measuring **circuit**. (6pp)o

79/3,AB/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

02313052
MIS TYPE SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE

PUB. NO.: 62-229952 [JP 62229952 A]
PUBLISHED: October 08, 1987 (19871008)
INVENTOR(s): MATSUKI KOJI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-072855 [JP 8672855]
FILED: March 31, 1986 (19860331)
JOURNAL: Section: E, Section No. 594, Vol. 12, No. 99, Pg. 67, March 31, 1988 (19880331)

ABSTRACT

PURPOSE: To obtain the MIS type semiconductor **integrated circuit** device provided with a monitoring **transistor** with which an 1.mu.AVth and an externally inserted Vth can be made to have an equal value by a method wherein the monitoring **transistor**, on which the ratio of the width and length of a channel is set in such a manner that the voltage (1.mu.AVth) between a gate and a source will be made equal to the threshold voltage (externally inserted Vth), is provided.

CONSTITUTION: The drain and source of an **MOS transistor** Q1 are connected to the drain and source of a P-channel type **MOS transistor** Q2, and a pad 14 is connected to these gates respectively. The **W**/L of the N-channel type **MOS transistor** Q1 is set at 40/4, for example, and the **W**/L of the above- mentioned P-channel type **MOS transistor** Q2 is set at 20/4, for example. In other words, the size of said **transistors** is set corresponding to the ratio of the (gm) of the N-cannel type **MOS transistor** Q1 and the (gm) of the P-channel. type **MOS transistor** Q2. As a result, the 1.mu.AVth and the externally inserted Vth are made equal.

79/3,AB/4 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

01200664
SEMICONDUCTOR DEVICE AND ITS EVALUATING METHOD

PUB. NO.: 58-138064 [JP 58138064 A]
PUBLISHED: August 16, 1983 (19830816)
INVENTOR(s): IWAI HIROSHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-020118 [JP 8220118]
FILED: February 10, 1982 (19820210)
JOURNAL: Section: E, Section No. 209, Vol. 07, No. 251, Pg. 102, November 08, 1983 (19831108)

ABSTRACT

PURPOSE: To form a TEG consisting of a large number of fundamental characteristic evaluating elements without lowering the degree of integration by forming a plurality of the evaluating elements and a pad section into a LSI chip.

CONSTITUTION: The source 13 of a **MOS transistor** 16(sub 1) is connected to the pad section 18(sub 1) for first measurement, the drain 14 of the **transistor** to the pad section 18(sub 2) for second measurement and a gate **electrode** 15 to the pad section 18(sub 3) for third measurement respectively by trimming a first **Al** main wiring 20(sub 1) section between first and second **Al** branch wiring 19(sub 1), 19(sub 2) connected to the source 13 and the drain 14 by laser beams. A probe card, etc. are connected to the pad sections 18(sub 1)-18(sub 3) for each measurement, and the electrical various characteristics of the specific **MOS transistor** 16(sub 1) are measured, thus evaluating the LSI chip.

80/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013269792
WPI Acc No: 2000-441698/200038
Related WPI Acc No: 1999-590926; 2000-387537; 2000-411439; 2000-422572; 2000-441625; 2000-441788; 2000-543297; 2001-080143; 2001-080152; 2001-373481; 2001-463808; 2001-541126; 2001-588757; 2002-009590; 2002-009898; 2002-178428; 2002-224340; 2002-237900; 2002-253707; 2002-267085; 2002-381791; 2002-424553; 2002-425165
XRPX Acc No: N00-329642
Node voltage control for high speed communication IC, comprises preventing input signal from passing via transmission gate by pulling node to fixed voltage, when gate is closed in response to clock signal
Patent Assignee: BROADCOM CORP (BROA-N)
Inventor: HATAMIAN M
Number of Countries: 091 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6411117	B1	20020625	US 98108319	P	19981113	200246
			US 98108647	P	19981116	

Priority Applications (No Type Date): US 99130616 P 19990422; US 98108319 P 19981113; US 98108647 P 19981116; US 99439120 A 19991112
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6411117	B1			G01R-031/26	Provisional application US 98108319
					Provisional application US 98108647
					Provisional application US 99130616

Abstract (Basic): WO 200029860 A2
Abstract (Basic):
NOVELTY - The node (P1) is driven with an input signal, when a **CMOS** type transmission gate (504) is open during the first steady state clock signal to allow the input signal to pass from the input terminal to the output terminal. When the transmission gate is closed during the second steady state of the clock signal, the node is pulled to a fixed voltage to prevent the input signal from passing through the gate.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a node voltage controlling system.
USE - For controlling the voltage at a node in the dynamic register of a high speed communication **integrated circuit**, e.g. a gigabit transceiver chip of a gigabit ethernet used for high speed LAN communication, or a multi-pair communication system.
ADVANTAGE - Enables control of voltage at the node in a dynamic register to prevent the node from having an unknown floating voltage during steady state of a clock signal.
DESCRIPTION OF DRAWING(S) - The figure shows a schematic diagram of rising edge **CMOS** dynamic register with IDDQ testing capability.
CMOS type transmission gate (504)
Node (P1)
pp; 36 DwgNo 5/6

80/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004075390
WPI Acc No: 1984-220931/198436
XRPX Acc No: N84-165118
Moving-charge monitor for **MOS integrated circuit** - applies simultaneous thermal and electrical stresses to multiple test points
Patent Assignee: COMMISSARIAT ENERGIE ATOMIQUE (COMS); TOKYO ELECTRON LTD (TKEL); TOSHIBA KK (TOKE)
Inventor: HARTMANN J; JEUCH P; HASEGAWA I; HIRANO Y; HORIOKA K; MATSUSHITA T; OGASAWARA M; TAHARA Y
Number of Countries: 009 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 117810	A	19840905	EP 84400338	A	19840217	198436	B
FR 2541779	A	19840831				198440	
JP 59163833	A	19840914	JP 8432759	A	19840224	198443	
EP 117810	B	19870506				198718	
DE 3463573	G	19870611				198724	
US 4672313	A	19870609	US 84580840	A	19840216	198725	
US 5356515	A	19941018	US 91779376	A	19911018	199441	
			US 92988809	A	19921210		

Priority Applications (No Type Date): FR 833046 A 19830224; JP 90283155 A 19901019; JP 90300361 A 19901105; JP 91352074 A 19911213; JP 91331077 A 19911216
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 117810	A	F	12		
Designated States (Regional): CH DE GB IT LI NL					
EP 117810	B	F			
Designated States (Regional): CH DE FR GB IT LI NL					
US 5356515	A		23	H01L-021/00	CIP of application US 91779376 patent EP 117810 patent JP 5166770 CIP of patent US 5302236

Abstract (Basic): EP 117810 A

A Si wafer (14) carrying the **integrated circuits** to be tested is held by vacuum aspiration (16) on a base (10) equipped with an electric heating element (12) for thermal stressing. Electrical stress is applied from an upper conductor (30a) through a package (20) and a conductive film (18) e.g. of stainless steel or **Al**- or **Cu**-coated plastic to the upper surface of the wafer (14), while a lower conductor (30b) applies a potential to the under surface through the conductive base (10).

The film (18) is forced against the upper surface by compressed air (28) in the cavity (24) of the package (20) at a pressure of a few tenths above 1 atmos. Alternatively the cavity (24) may be open to atmos. and the film (18) held by vacuum in an enclosed annular space

around the wafer (14).
USE - For controlling **MOS circuit** mfr.
Dwg.2/3

Abstract (Equivalent): EP 117810 B
Device for checking moving electrical charges in an **MOS** technology **integrated circuit** comprising a chip support (10) provided with a means of heating (12), means of fixing an **integrated circuits** chip made from silicon on the chip support (10), at least one means of electrical contact (8) for applying an electrical voltage to the points of the **integrated circuits** to be tested, a means of bias (30a and 30b) applying a potential difference between the two faces of the silicon chip (14) carrying the **integrated circuits** by means of two **electrodes**, each in contact with one of the faces of the silicon chip (14), characterised in that the first **electrode** is formed from a conductive membrane (18) covering the silicon chip (14), this first **electrode** being held in contact with the silicon chip (14) by a difference in pressure between its two faces, the second **electrode** being formed by the chip support (10) which is electrically conductive.
(6pp

80/3,AB/3 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06641640
TESTING DEVICE FOR CAPACITOR IN **INTEGRATED CIRCUIT** AND METHOD THEREOF

PUB. NO.: 2000-227454 [JP 2000227454 A]
PUBLISHED: August 15, 2000 (20000815)
INVENTOR(s): ITAGAKI ISAO
APPLICANT(s): NEC YAMAGATA LTD
APPL. NO.: 11-026771 [JP 9926771]
FILED: February 03, 1999 (19990203)

ABSTRACT

PROBLEM TO BE SOLVED: To easily test performance of a capacitor in an **integrated circuit** by indicating an impressed voltage in impression of voltage to a dielectric body of a capacitor in the **integrated circuit** and detecting current flowing through the dielectric body for indicating it.

SOLUTION: A testing device for a capacitor in an **integrated circuit** is constructed of a voltage impression display device 1 and a current detection display device 2. The voltage impression display device 1 impresses voltage to a **silicon nitride** film 6 serving as a dielectric body for a **MOS** type capacitor 3, and at the same time, indicates the impressed voltage, while the current detection display device 2 detects current flowing thorough the **silicon nitride** film 6 (dielectric body) and displays it. If impressed voltage is increased to a predetermined voltage when voltage is impressed to an anode A while a cathode B is grounded, electric current starts flowing. This electric current flow starting voltage (withstand voltage of the dielectric body) depends on a film thickness of the dielectric body. Dispersion of the film thickness of the dielectric body is a main factor of dispersion of a capacity value, so that a performance of the capacitor can be easily measured when a withstand voltage of the dielectric body is measured.

80/3,AB/4 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05584872
SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE AND METHOD OF INSPECTION

PUB. NO.: 09-199672 [JP 9199672 A]
PUBLISHED: July 31, 1997 (19970731)
INVENTOR(s): KOIKE NORIO
APPLICANT(s): MATSUSHITA ELECTRON CORP [000584] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-009081 [JP 969081]
FILED: January 23, 1996 (19960123)

ABSTRACT

PROBLEM TO BE SOLVED: To remove defective chips on a semiconductor wafer in a lump burning-in of the semiconductors at wafer state by connecting a first and a second **electrodes** and wiring to each branch line of conductor lines that comprise three branch lines and the branch lines connected to the wiring comprise fuses.

SOLUTION: A first and a second **electrodes** 2 and 3 of pad **electrodes** and wiring 4 that is connected to an internal **circuit** are provided on an **integrated circuit** chip 1. The first and the second **electrodes** 2 and 3 and the wiring 4 are connected to each branch line of a conductor line 5 that comprises three branch lines that are extended branching in three directions. The branch line connected to the wiring 4 comprises a fuse 9 made of **Al** and a part of **Al** wiring 8 that is connected serially. The fuses are blown for the defective chips by supplying power of more than the maximum allowable power to the first and the second **electrodes** 2 and 3 and the power supply to the inside **circuit** is stopped. With this, the effect from the defective chips at the lump burning-in of the semiconductor chips in the wafer state can be avoided.

80/3,AB/5 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

04853726
SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE

PUB. NO.: 07-146326 [JP 7146326 A]
PUBLISHED: June 06, 1995 (19950606)
INVENTOR(s): FURUKAWA CHIAKI
YAMAMOTO TAKAHIRO
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
FUJITSU VLSI LTD [491219] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-295627 [JP 93295627]
FILED: November 25, 1993 (19931125)

ABSTRACT

PURPOSE: To easily change the timing of an internal control signal by using an external signal and to shorten the time required for analyzing the timing.

CONSTITUTION: A power supply voltage Vcc is supplied to the internal **circuit** 1 of a semiconductor **integrated circuit** device and the **circuit** 1 is driven on the basis of an internal control signal **Sin**. A voltage detecting **circuit** 2 is connected to an external input terminal 5 and inputs external signals of voltages higher than the voltage Vcc supplied to the **circuit** 1. The **circuit** 2 outputs the load generating signal H corresponding to the voltage of the inputted external signals to a load generating **circuit** 3. The **circuit** 3 gives a load to a timing adjusting **circuit** 4, inputs the signal H, and generates a load having the magnitude corresponding to the signal H. The **circuit** 4 delays the control signal **Sin** by using the load of the **circuit** 3 and outputs the delayed signal **Sin** to the internal **circuit** 1

80/3,AB/6 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

04523634
LATCH UP MEASURING METHOD OF **INTEGRATED CIRCUIT** AND VOLTAGE GENERATION **CIRCUIT** USING THE SAME

PUB. NO.: 06-167534 [JP 6167534 A]
PUBLISHED: June 14, 1994 (19940614)
INVENTOR(s): KOKUBO SHIGERU
NAKAYA TOSHIYUKI
APPLICANT(s): HANWA DENSHI KOGYO KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-116620 [JP 92116620]
FILED: March 25, 1992 (19920325)
JOURNAL: Section: P, Section No. 1801, Vol. 18, No. 497, Pg. 70, September 16, 1994 (19940916)

ABSTRACT

PURPOSE: To enable latch up measurement free from the effect of a floating inductance by applying a voltage by a specified waveform to terminals of an IC.

CONSTITUTION: In connection to voltage sources 21-24 ranging voltages V(sub 1)-V(sub 4) with a relay sequentially according to time T(sub 1)-T(sub 4) a voltage waveform is obtained automatically. The latch up measurement of an IC is based on changing the voltages V(sub 1)-V(sub 4) and the time T(sub 1)-T(sub 4). Values of the voltages V(sub 2) and V(sub 3) and the time T(sub 2) and T(sub 3) are set so as to **al** low the generation of a latch up according to the IC to be tested and a terminal voltage and thereafter, a voltage value and application time approximate to the values are detected. This eliminates the charging of a capacitor with an electric charge and hence, there is no eventual deficiency, for example, variations in the results of testing or each measurement with no effect of a floating inductance thereby stabilizing a latch up reference value.

80/3,AB/7 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

01835976
SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE

PUB. NO.: 61-050076 [JP 61050076 A]
PUBLISHED: March 12, 1986 (19860312)
INVENTOR(s): MOBARA HIROSHI
IZEKI HIDEMI
SATO KOICHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
TOSHIBA MICRO COMPUT ENG CORP [486761] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-172558 [JP 84172558]
FILED: August 20, 1984 (19840820)
JOURNAL: Section: P, Section No. 479, Vol. 10, No. 210, Pg. 135, July 23, 1986 (19860723)

ABSTRACT

PURPOSE: To enable the measurement of characteristics of a **circuit** to be measured within an IC without putting a **gold** wire thereon, by controlling an analog switch connected to an input/output terminal of an analog **circuit** section from outside.

CONSTITUTION: When measuring characteristics of bandpass filters 11(sub 1)-11(sub 4) for spectral analysis of an input signal IN by the frequency band, linear elements S(sub 1), S(sub 3), S(sub 3) and S(sub 4) are set for conducting state and other linear elements for high output impedance state by a control signal CS and a test signal is inputted from an input terminal 14 to obtain outputs an external terminals 15(sub 1)-15(sub 4). On the other hand, when measuring rectifier **circuits** 12(sub 2) and 12(sub 4), linear elements S(sub 2), S(sub 7), S(sub 5) and S(sub 8) are set for conducting state and a test signal is supplied from external terminals 15(sub 1) and 15(sub 3) to obtain outputs at external terminals 15(sub 2) and 15(sub 4). When measuring a lowpass filter 13(sub 4), linear elements S(sub 8) and S(sub 9) are set for conducting state and a test signal is supplied from the external terminal 15(sub 4) to obtain the output thereof at the external terminal 15(sub 3).

88/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014546806
WPI Acc No: 2002-367509/200240
XRPX Acc No: N02-286955
Probe for testing **integrated circuit** chips, has several needles integrally provided to electroconductive cords made of material same as that of needles, which include wires **coated** with **insulation** material
Patent Assignee: CITIZEN WATCH CO LTD (CITL)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2002055118	A	20020220	JP 2000243587	A	20000811	200240	B

Priority Applications (No Type Date): JP 2000243587 A 20000811
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002055118	A		5	G01R-001/073	

Abstract (Basic): JP 2002055118 A
Abstract (Basic):
NOVELTY - The probe has several needles (3) integrally provided to electroconductive cords (2) made of material same as that of needles, which contact the material (7) under test. The needle has a wire made of **copper** silver-alloy material integrally provided to the cord, **coated** with **insulation** material except at the tip. A guide board with insertion holes for needles, moves the needles axially towards test material.
USE - To test the electrical property of **integrated circuit** (IC) chip, **printed circuit** board.
ADVANTAGE - As the probe needle and the electroconductive cord are integrally formed, the failure of a connection portion is eliminated and a reliable probe is obtained at a low cost.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the probe. (Drawing includes non-English language text).
Electroconductive cords (2)
Needles (3)
Material under test (7)
pp; 5 DwgNo 1/6

88/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014485424
WPI Acc No: 2002-306127/200235
XRPX Acc No: N02-239335
Manufacturing chip size package semiconductor device for producing high production yield and low cost using controlled adhesive sheet to fix chips
Patent Assignee: SONY CORP (SONY); NISHIYAMA K (NISH-I)
Inventor: NISHIYAMA K
Number of Countries: 029 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1152464	A2	20011107	EP 2001110351	A	20010426	200235	B
US 20020004288	A1	20020110	US 2001843630	A	20010427	200235	
JP 2001313350	A	20011109	JP 2000130001	A	20000428	200235	
KR 2001104643	A	20011126	KR 200123171	A	20010428	200235	

Priority Applications (No Type Date): JP 2000130001 A 20000428
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1152464	A2	E	24	H01L-023/31	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
US 20020004288	A1			H01L-021/66	
JP 2001313350	A		13	H01L-023/12	
KR 2001104643	A			H01L-023/12	

Abstract (Basic): EP 1152464 A2
Abstract (Basic):
NOVELTY - Solder paste is formed by a wet back method to form a solder bump (16) using nickel **electrode**-less plating or solder paste screen **printing** and flux and residual paste are then removed. Non-defective large-scale integration chips (4) are positioned onto the transport substrate to form a pseudo-wafer with only non-defective chips set equidistantly apart, covered by a **silicon dioxide film** (11) and a passivation film (12).
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for a chip-like electronic component and for a pseudo-wafer.
USE - Manufacturing chip-like electronic component.
ADVANTAGE - Minimizing damage caused by grinding bottom surface.
DESCRIPTION OF DRAWING(S) - The drawing shows a fabrication step
Solder bump (16)
Chip (4)
Insulating film (11)
Passivation film (12)
pp; 24 DwgNo 1J/12

88/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013637905
WPI Acc No: 2001-122113/200113
XRAM Acc No: C01-035344
XRPX Acc No: N01-089602

Improved impedance-matched interconnection device for connecting vertical-pin **integrated circuit** probing device to **integrated circuit** test equipment comprises **printed circuit** test board, mounting plate, and space transformer

Patent Assignee: WENTWORTH LAB INC (WENT-N)
Inventor: MARTEL A P; MCQUADE F T

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6160412	A	20001212	US 98186084	A	19981105	200113	B

Priority Applications (No Type Date): US 98186084 A 19981105
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6160412	A		11	G01R-031/02	

Abstract (Basic): US 6160412 A
Abstract (Basic):

NOVELTY - An improved impedance-matched interconnection device comprises a mounting plate attached to the **printed circuit** test board having PCB traces adapted to be connected in test **circuit** relationship to the **integrated circuit** test equipment; and a laminated impedance-matched space transformer comprising a conductive ground plane **layer**, a **dielectric layer**, and a conductive trace layer.

DETAILED DESCRIPTION - An improved impedance-matched interconnection device comprises a **printed circuit** test board (PCB); a mounting plate (48) attached to the PCB (44) having a pressure plate portion (48a) with a flat lower surface extending into the aperture; and a laminated impedance-matched space transformer (54) comprising a conductive ground plane **layer**, a **dielectric layer**, and a conductive trace layer. The PCB has PCB traces adapted to be connected in test **circuit** relationship to the **integrated circuit** test equipment. The PCB traces are arranged around the aperture (44a) to define a large outer connection pattern. The conductive ground plane layer is in contact with the flat surface of the pressure plate portion. The **dielectric layer** is adhered to the ground plane layer and the conductive trace layer is adhered to the **dielectric layer**. The trace **layer** comprises space transformer traces. The selected space transformer traces have contact terminals arranged in a second small inner connection pattern adapted to make temporary contact on one side of the traces with respective exposed heads of the vertical-pin probes (18) in the first small inner connection pattern and having respective ends extending beyond the edge of the ground plane layer and electrically

connected on the other side of the traces to respective PCB traces of the large outer connection pattern. The impedance-matched interconnector repetitively connects a vertical-pin **integrated circuit** probing device to **integrated circuit** test equipment. The probing device is of a type having conductive metal vertical-pin probes with exposed heads on the upper side of the probing device defining a first small inner connection pattern.

USE - For connecting a vertical-pin **integrated circuit** probing device to **integrated circuit** test equipment.

ADVANTAGE - Improved interconnection device for connecting a vertical-pin **integrated circuit** probing device to external **integrated circuit** test equipment. Improved impedance-matched space transformer for connecting a vertical-pin **integrated circuit** probing device to a **printed circuit** board. Improved space transformer of laminated construction which simplifies impedance-matching, adjustability for alignment, and improved connection to the **printed circuit** test board.

DESCRIPTION OF DRAWING(S) - The figure shows an exploded perspective view of the interconnection device.

vertical-pin probes (18)

08/13/2002 09/813,087

88/3,AB/4 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06645122
CONTACT PROBE EQUIPED WITH **TUNGSTEN** NEEDLE AND PROBE DEVICE

PUB. NO.: 2000-230938 [JP 2000230938 A]
PUBLISHED: August 22, 2000 (20000822)
INVENTOR(s): ASO TAKESHI
KATO NAOKI
YOSHIDA HIDEAKI
IWAMOTO TAKAFUMI
APPLICANT(s): MITSUBISHI MATERIALS CORP
APPL. NO.: 11-030696 [JP 9930696]
FILED: February 08, 1999 (19990208)

ABSTRACT

PROBLEM TO BE SOLVED: To make adjustable a characteristic impedance with use of a **tungsten** needle, and reduce external noises and signal losses at high frequencies.

SOLUTION: Base parts 6b... of a plurality of **tungsten** needles 6... are soldered to **electrodes** of a **printed** board. Middle parts are fixed to a holding part 16 and leading end parts 6a are curved. A double-layer film 20 is applied via an adhesive from each of the base parts 6b... of the **tungsten** needles 6... to the holding part 16, thereby constituting a contact probe 14. The double-layer film 20 is comprised of an **insulating** resin **film** 22 and a grounded metallic film 24 of a good conductivity. The contact probe 14 constitutes a microstrip line.

88/3,AB/5 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

04745343
PROBE DEVICE

PUB. NO.: 07-037943 [JP 7037943 A]
PUBLISHED: February 07, 1995 (19950207)
INVENTOR(s): SANO KUNIO
APPLICANT(s): TOKYO ELECTRON LTD [367410] (A Japanese Company or Corporation), JP (Japan)
TOKYO ELECTRON YAMANASHI KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-200023 [JP 93200023]
FILED: July 19, 1993 (19930719)

ABSTRACT

PURPOSE: To provide a prober, in which a conductive protrusion used as a contact in a probe card is adequately put in contact with an **electrode** pad in a chip.

CONSTITUTION: A movable plate 4 facing to a wafer stage 2 and a link arm 43 are provided so that the movable plate 4 kept in parallel with the wafer (**W**) can be rotated around an axis in parallel with the wafer (**W**). A flexible multilayer interconnection board 31 having bumps (conductive protrusions) 32 put in a row is mounted on the rear face of the movable plate 4. Both ends of the wiring board 31 is fixed to a **printed** board on the upper side. In this constitution, the wiring board 31 is pushed downward by a buffer body 44 in a notch part 41 that passes through the movable plate 4. when the wafer (**W**) abuts on the bump 32 and moves upward, the bump 32 pushes the **electrode** pad and slides sideways through rotating force of the movable plate 4 as well as restoring force of the buffer body 44. Then, the bump 32 abrades a natural **oxide film** on a surface of the **electrode** pad.

88/3,AB/7 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

01842881
SEMICONDUCTOR INSPECTING DEVICE

PUB. NO.: 61-056981 [JP 61056981 A]
PUBLISHED: March 22, 1986 (19860322)
INVENTOR(s): MATAI SADAO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-178034 [JP 84178034]
FILED: August 27, 1984 (19840827)
JOURNAL: Section: P, Section No. 482, Vol. 10, No. 220, Pg. 112, July 31, 1986 (19860731)

ABSTRACT

PURPOSE: To enable accurate testing of electric characteristics employing a high frequency signal, by arranging a probe of a probe card in an coaxial probe structure to prevent reflection of the high frequency signal with the matching of the impedance at the probe section.

CONSTITUTION: An **insulation layer** 7 made of teflon or the like is formed at a specified thickness on the circumference of a probe 6 of a probe card used for the inspection of a semiconductor wafer. Then, a conductive layer 8 is formed on the **insulation layer** 7 by evaporation of **copper** or aluminum to be made in a coaxial probe structure. The probe 9 thus obtained is cut off at the part of the **insulation layer** 7 and at the part of the conductive layer 8 at the front and rear ends thereof in a fixed range to be set on a **printed circuit** board 1, bent by a specified angle at the tip 9a intended to contact an **electrode** section of a semiconductor device and then, arranged on a metalic base 5b with the rear end 9b thereof connected to a wire pattern 3. Then, the metalic base 5b is fixed to a gland layer 11 on the **printed circuit** board 1 with the a conductive adhesive.

97/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014386394
WPI Acc No: 2002-207097/200227
XRPX Acc No: N02-157768
In-**circuit** test adaptors, includes double sleeve with optimal test spring contacts through which the test terminals of a PCB is directly connected to a test system
Patent Assignee: BOCTOR G (BOCT-I); RATZKY B (RATZ-I)
Inventor: BOCTOR G; RATZKY B
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 10016453	A1	20011115	DE 1016453	A	20000401	200227	B

Priority Applications (No Type Date): DE 1016453 A 20000401
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 10016453	A1		10	G01R-031/28	

Abstract (Basic): DE 10016453 A1
Abstract (Basic):
NOVELTY - A **printed circuit** board has its test terminals directly connected to a test system via the optimal test spring contacts of a double sleeve. The PCB is prefabricated with a **copper** layer on which the test terminals are strategically formed.
USE - In-**circuit** test adaptors.
ADVANTAGE - Reduces interferences during actual testing by determining the shortest conduction **paths**.
DESCRIPTION OF DRAWING(S) - The figure shows the test adaptor structure. (Drawing includes non-English language text)
pp; 10 DwgNo 1/5

97/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013940216
WPI Acc No: 2001-424430/200145
XRAM Acc No: C01-128380
XRPX Acc No: N01-314806
Contact structure for establishing electrical connection with contact targets, e.g. contact pads of electronic devices, has contactors formed on the substrate through microfabrication process
Patent Assignee: ADVANTEST KK (ADVA-N)
Inventor: FRAME J W; KHOURY T A
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6250933	B1	20010626	US 2000488661	A	20000120	200145	B
DE 10101538	A1	20010802	DE 1001538	A	20010115	200145	
JP 2001284421	A	20011012	JP 200144302	A	20010117	200176	
KR 2001076422	A	20010811	KR 20013401	A	20010120	200213	

Priority Applications (No Type Date): US 2000488661 A 20000120
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6250933	B1		25	H01R-012/00	
DE 10101538	A1			G01R-031/28	
JP 2001284421	A		17	H01L-021/66	
KR 2001076422	A			H01R-012/00	

Abstract (Basic): US 6250933 B1
Abstract (Basic):
NOVELTY - A contact structure includes dielectric substrate (20) with depression, and contactors (30) having a bridge like shape formed on the substrate through a microfabrication process. The contactors are formed with a horizontal portion that produces a contact force when the contactor is pressed against a contact target.
DETAILED DESCRIPTION - A contact structure includes dielectric substrate with a depression, and contactors having a bridge like shape formed on the substrate through a microfabrication process. The contactors are formed with a horizontal portion having two angled portions connected to the dielectric substrate. The horizontal portion has a free end positioned over the depression on the dielectric substrate. The horizontal portion of the contactor produces a contact force when the contactor is pressed against a contact target such that the horizontal portion enters the depression while exerting the contact force.
USE - The contact structure is for establishing electrical connection with contact targets such as contact pads or leads of electronic **circuits** or devices. It is also used in **integrated circuit** packaging. It is particularly to be used in a probe card to test semiconductor wafers, semiconductor chips, packaged semiconductor devices, module sockets, **printed circuit** boards

97/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013853927
WPI Acc No: 2001-338140/200136
XRAM Acc No: C01-104913
XRPX Acc No: N01-244246
Anisotropic conductive sheet for electrical connection to electronic components/connector for **printed circuit** substrate/semiconductor **integrated circuit** to be tested
Patent Assignee: JSR CORP (JAPS)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001067942	A	20010316	JP 99244667	A	19990831	200136	B

Priority Applications (No Type Date): JP 99244667 A 19990831
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001067942	A		15	H01B-005/16	

Abstract (Basic): JP 2001067942 A
Abstract (Basic):
NOVELTY - An anisotropic conductive sheet contains conductive particles in an elastic base material.
DETAILED DESCRIPTION - The elastic base material has a fluorinated polyether skeleton in a molecular structure. The terminal of the molecular structure is formed of the hardened product of liquid fluorocarbon rubber having a silicone crosslinking reaction group.
USE - The anisotropic conductive sheet is used for electrical connection to electronic components, a connector for a **printed circuit** substrate, a semiconductor **integrated circuit** to be tested.
ADVANTAGE - The anisotropic conductive sheet is prevented from adhesion to a body to be connected or has depressed adhesion to the body to be connected even if the anisotropic conductive sheet is pressed by the body to be connected and is left behind for a long period of time at high temperatures. In separating the anisotropic conductive sheet from the **circuit** device to be tested, no damage is observed. The resulting anisotropic conductive sheet has prolonged service life.

97/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013794248
WPI Acc No: 2001-278459/200129
XRAM Acc No: C01-084697
XRPX Acc No: N01-199579
Anisotropic conductive sheet for electric connection between **circuit** apparatuses, contains electroconductive particles in elastic polymeric material and has predefined permanent compression deformation
Patent Assignee: JSR CORP (JAPS)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001067940	A	20010316	JP 99237908	A	19990825	200129	B

Priority Applications (No Type Date): JP 99237908 A 19990825
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001067940	A		10	H01B-005/16	

Abstract (Basic): JP 2001067940 A
Abstract (Basic):
NOVELTY - An anisotropic conductive sheet (10) contains electroconductive particles in an elastic polymeric material consisting of cured substance of addition type liquid silicone rubber. The sheet has permanent compression deformation of 15% at 150degreesC.
USE - For electric connection between **circuit** apparatuses such as **printed circuit** board, semiconductor **integrated circuits** of electronic components.
ADVANTAGE - Electroconductivity of the sheet is maintained for long period of time, therefore high thermal durability is attained. Generation of deformation on the base material is inhibited even when used continuously.
DESCRIPTION OF DRAWING(S) - The figure shows sectional drawing of the anisotropic conductive sheet. (Drawing includes non-English language text).
Anisotropic conductive sheet (10)

97/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010573842
WPI Acc No: 1996-070795/199608
XRPX Acc No: N96-059414
Indicating locations of defective and good devices on semiconductor wafer - fixing label bearing data onto narrow area of wafer surface on which no device is fabricated
Patent Assignee: NEC CORP (NIDE); NEC KYUSHU LTD (KYUN)
Inventor: NISHIMURA K
Number of Countries: 003 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2291739	A	19960131	GB 9514920	A	19950720	199608	B
JP 8037210	A	19960206	JP 94170613	A	19940722	199615	
US 5705935	A	19980106	US 95505623	A	19950721	199808	
GB 2291739	B	19980812	GB 9514920	A	19950720	199834	

Priority Applications (No Type Date): JP 94170613 A 19940722
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2291739	A		31	H01L-021/66	
JP 8037210	A		6	H01L-021/66	
US 5705935	A		10	G01R-031/02	
GB 2291739	B			H01L-021/66	

Abstract (Basic): GB 2291739 A

Mapping date indicative of locations of acceptable and/or defective **integrated circuits** are **printed** on a label sheet (12g). The label sheet is bonded to a peripheral area of a semiconductor wafer (10).

Data may be in the form of first marks indicating first sub-areas of the wafer surface of either acceptable or defective products, and a second mark indicative of a reference for determining the first sub-area, the label being fixe to a second sub-area surface.

ADVANTAGE - Does not prejudice production yield, e.g. caused by **aluminium** particles.

Dwg.8/8

97/3,AB/12 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06075547
BGA PACKAGE, TEST SOCKET THEREFOR AND TEST FOR BGA PACKAGE

PUB. NO.: 11-017058 [JP 11017058 A]
PUBLISHED: January 22, 1999 (19990122)
INVENTOR(s): YAMASHITA MASAMICHI
APPLICANT(s): NEC CORP
APPL. NO.: 09-170043 [JP 97170043]
FILED: June 26, 1997 (19970626)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a ball grid array(BGA) package, a test socket therefor and a method for testing the BGA package, which can avoid the influences of an interval and area of inspection pads, even when the size of soldering bumps and the interval of the bumps in the BGA package are made small.

SOLUTION: An IC chip 11 is mounted on a front surface of a **printed circuit** board 12 and is connected with wiring lines 13 (on the front side of the board) on the board 12 by bonding wires 16. The wiring lines 13 on the board 12 are connected through a through hole 14 to the wiring lines 13 (on the rear side of the board) on the board, which lines are connected with soldering bumps 15. Further, the wiring lines on the front side of the board 12 are extended up to side faces of the board 12, on which extended wiring lines an Ni plated layer 19 and an **Au** plated layer 20 are formed. These plated layer parts are electrically connected with **electrode** pads 11a of the chip 11 through the soldering bumps 15, board rear-side wiring lines 13, through-hole 14, board front-side wiring lines 13 and bonding wires 16 respectively, and act as inspection pads.

97/3,AB/14 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

05128325
PROBE EQUIPMENT

PUB. NO.: 08-083825 [JP 8083825 A]
PUBLISHED: March 26, 1996 (19960326)
INVENTOR(s): SANO KUNIO
APPLICANT(s): TOKYO ELECTRON LTD [367410] (A Japanese Company or Corporation), JP (Japan)
TOKYO ELECTRON YAMANASHI KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-215870 [JP 94215870]
FILED: September 09, 1994 (19940909)

ABSTRACT

PURPOSE: To bring a contactor of probe equipment into contact with an **electrode** pad without fail.

CONSTITUTION: Probe equipment has a setting stage 13 for a semiconductor wafer **W** and a **printed** wiring board 42 is provided above the stage. A flexible film-like probe card 12 is fitted to the **printed** wiring board 42. The probe card 21 has a main region 27 wherein a contactor 28 to be brought into contact with an **electrode** pad EP of the wafer **W** is disposed. A hard rectangular frame 29 for giving flatness is joined on the rear side of the probe card 21. An extensible chamber 54 for bringing the contactor 28 into elastic contact with the **electrode** pad EP of the wafer **W** is provided on the rear side of the probe card 21. Between the extensible chamber 54 and the probe card 21, a pressing plate 55 having a hard base and an elastic layer is provided. By the pressing plate 55, the main region 27 is pressed out toward the wafer **W** in parallel thereto.

97/3,AB/15 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

05128324
PROBE EQUIPMENT

PUB. NO.: 08-083824 [JP 8083824 A]
PUBLISHED: March 26, 1996 (19960326)
INVENTOR(s): YAMADA MASAYUKI
APPLICANT(s): TOKYO ELECTRON LTD [367410] (A Japanese Company or Corporation), JP (Japan)
TOKYO ELECTRON YAMANASHI KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-215869 [JP 94215869]
FILED: September 09, 1994 (19940909)

ABSTRACT

PURPOSE: To bring a contactor of probe equipment into contact with an **electrode** pad without fail.

CONSTITUTION: Probe equipment has a setting stage 13 for a semiconductor wafer **W** and a **printed** wiring board 42 fitted with a support block 50 is provided above the stage. A flexible film-like probe card 21 is fitted so that it covers a recessed part 55 of the support block 50. The probe card 21 has a main region 27 wherein a contactor 28 to be brought into contact with an **electrode** pad EP of the wafer **W** is disposed. A hard rectangular frame 29 for giving flatness is joined on the rear side of the probe card 21. A pusher 71 is provided inside the recessed part 55 of the support block 50 and it comes into contact with the rear side of the probe card 21. The pusher 71 is disposed swingably at the lower end of the shaft 74 supported vertically. The shaft 74 is supported by the support block 50 through the intermediary of two coned disk springs 77 and 78.

97/3,AB/16 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

04281537
PROBE CARD

PUB. NO.: 05-273237 [JP 5273237 A]
PUBLISHED: October 22, 1993 (19931022)
INVENTOR(s): YOKOTA KEIICHI
APPLICANT(s): TOKYO ELECTRON YAMANASHI KK [000000] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-100467 [JP 92100467]
FILED: March 26, 1992 (19920326)
JOURNAL: Section: P, Section No. 1681, Vol. 18, No. 45, Pg. 160, January 24, 1994 (19940124)

ABSTRACT

PURPOSE: To prevent a probe needle from slipping down even when it is in touch with an **electrode** or a terminal as a result of the shift of the central position, by forming an end part of the probe needle to be linearly in touch with the **electrode** part of a semiconductor device.

CONSTITUTION: A probe card 1 consists of a **printed circuit** board and a probe needle 3. A fixed end of the probe needle is fixed to the substrate, and a free end of the probe needle 3 is electrically in touch with an **electrode** of a semiconductor device for measurement. The probe neelde 3 is made of a wire material, e.g. **tungsten**. The fixed end of the wire material of the probe needle 3 is secured with a predetermined inclination to the surface of the substrate, and the end part of the wire to be in touch with a wafer 5 is bent with a predetermined inclination to a perpendicular line 6 to the surface of the wafer 5. A front end 3a of the probe needle 3 is notched at the height .delta.t in parallel to the surface of the wafer 5 from an intersection P where the axis passing the end of the probe 3 intersects the perpendicular line 6.

Moreover, both sides of a front end face 3b of the notched probe neelde 3 are notched by predetermined angles .theta.(sub 1), .theta.(sub 2) in a manner to form a ridge.

97/3,AB/17 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

04071048
IC SOCKET

PUB. NO.: 05-062748 [JP 5062748 A]
PUBLISHED: March 12, 1993 (19930312)
INVENTOR(s): NISHINO TOMONORI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-218890 [JP 91218890]
FILED: August 29, 1991 (19910829)
JOURNAL: Section: E, Section No. 1397, Vol. 17, No. 375, Pg. 41, July 14, 1993 (19930714)

ABSTRACT

PURPOSE: To prevent the deformation of a lead by **integrating** a **circuit** board provided with a protruded **electrode** in response to the pitch of the external terminal lead of a semiconductor device with an IC socket, using the **electrode** as a contact piece with the lead, and arranging a spring individually pressing the lead on the socket pressing plate side.

CONSTITUTION: A mold presser 19 formed on each IC pressing plate 4, a semiconductor device 5, a double-sided **printed circuit** board 13, and the second **printed circuit** board 23 are molded with their centers matched respectively, an opening section 12 is provided at the center section of the board 13 so that the lower face of the resin seal section of the device 5 does not interfere with the upper face of the board 13, and a protruded **electrode** 14 formed on the upper face of the board 3 and an **electrode** pad 21 formed on its back face are conducted via a **Cu** pattern 18 and a through hole 17. The second board 23 is used as a relay board for the burn-in test and measurement of the device 5. A lead 6 is pinched by the **electrode** 14 and a spring 20 buried in the pressing plate 4, and the contact is improved without deforming the lead 6.

97/3,AB/18 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO

04048448
CHARACTERISTIC INSPECTION DEVICE OF SEMICONDUCTOR DEVICE

PUB. NO.: 05-040148 [JP 5040148 A]
PUBLISHED: February 19, 1993 (19930219)
INVENTOR(s): ISHIKAWA OSAMU
OTA TOSHIMICHI
MAEDA MASAHIRO
AZUMA CHINATSU
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-199371 [JP 91199371]
FILED: August 08, 1991 (19910808)
JOURNAL: Section: P, Section No. 1561, Vol. 17, No. 329, Pg. 159, June 22, 1993 (19930622)

ABSTRACT

PURPOSE: To obtain a high-frequency characteristic inspection device of a semiconductor for amplifying power whose inspection accuracy is improved drastically.

CONSTITUTION: A module **printed-circuit** board 5 and a **printed-circuit** board 2 for evaluation which are soldered to a heat sink 11 are placed on a cooling block 1. A lead terminal 9 of the module is soldered and electrically connected while it is mounted on a wiring such as a micro strip line 4, etc., of the **printed-circuit** board 2 for evaluation. Also, a leg portion of the heat sink 11 is fixed to a cooling block 1. Input and output connectors 3 are mounted from the **printed-circuit** board 2 for evaluation and at the same time a bias supply terminal 10 is lead out and a DC bias is supplied to the module. A transistor 7 to be inspected is inserted into an opening 6 of the module **printed-circuit** board 5 and pressure is applied from an upper portion by using a lead press 12. thus enabling a **copper** foil 8 to be electrically connected to a transistor lead.

97/3,AB/21 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

02993579

MEASURING INSTRUMENT FOR SEMICONDUCTOR DEVICE

PUB. NO.: 01-291179 [JP 1291179 A]
PUBLISHED: November 22, 1989 (19891122)
INVENTOR(s): NAKAKOJI YOKI
APPLICANT(s): MATSUSHITA ELECTRON CORP [000584] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-121321 [JP 88121321]
FILED: May 18, 1988 (19880518)
JOURNAL: Section: P, Section No. 1004, Vol. 14, No. 72, Pg. 134, February 09, 1990 (19900209)

ABSTRACT

PURPOSE: To stably measure an electric characteristic in a high frequency area by sticking a **copper** plate to the outside periphery of a socket of a semiconductor to be measured, connecting one **electrode** of electronic parts to a socket part of a socket and connecting the other **electrode** to the **copper** plate.

CONSTITUTION: A **copper** plate 6 is stuck to the outside periphery of an IC socket for installing a semiconductor device to be measured 2 to a **printed** board 3. Also, a chip capacitor 7 is embedded into the outside periphery in the vicinity of a socket part 5, one **electrode** 7a of the capacitor 7 is connected to the socket part 5 by solder 8, and the other **electrode** 7b of the capacitor 7 is connected to the **copper** plate 6 by solder 8. Also, the **copper** plate 6 is connected to a ground terminal of the substrate 3 through a screw 9 for fixing the socket 1 to the substrate 3. In such a way, a wiring distance extending from a lead 4 of the device 2 to the ground terminal of the substrate 3 through the capacitor 7 becomes a distance (a + b + c) to the **copper** plate 6, and becomes about 1/3. Accordingly, an electric characteristic in a high frequency area can be measured stably.

97/3,AB/22 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO

02467233
PROBE CARD

PUB. NO.: 63-084133 [JP 63084133 A]
PUBLISHED: April 14, 1988 (19880414)
INVENTOR(s): MURATA YASUMICHI
APPLICANT(s): TOKYO ELECTRON LTD [367410] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 61-231011 [JP 86231011]
FILED: September 29, 1986 (19860929)
JOURNAL: Section: E, Section No. 651, Vol. 12, No. 320, Pg. 39, August 30, 1988 (19880830)

ABSTRACT

PURPOSE: To prevent a noise and a crsstalk by exposing the end of a coaxial cable 3mm or shorter to use it for a probe which is conducted with a high frequency signal of probes.

CONSTITUTION: One end is fixed to the lower side of a substrate 11 around the hole 12 of a **printed** substrate 11 of a probe card, the intermediate end is supported by a resin ring 13, and many probes 14 inclined downward to the center of the hole 12 are disposed. The probes 14 are connected to a terminal 15. A resin seat 17 and a coaxial cable connection socket 18 are provided on the **Au** plate 15 on the substrate 11. A coaxial probe 19 is buried by connecting the socket 18, and an **Au** annular plate 20 is disposed. The conductor exposed part 19d of the probe 19 is set to 3mm or shorted. A semiconductor wafer is disposed on the lower part of the hole 12, the probes 14 and the 19 are contacted with an **electrode** pad, a coaxial cable is connected to the socket 18, the cable and the terminal 15 are connected to a measuring instrument to be tested. According to this structure, a noise due to a high frequency signal and a crosstalk can be largely reduced to set the attenuation of the signal to -3dB or less at 5GHz.

97/3,AB/24 (Item 14 from file: 347)
DIALOG(R)File 347:JAPIO

00827771
MULTIPLE NEEDLE TYPE PROBE

PUB. NO.: 56-148071 [JP 56148071 A]
PUBLISHED: November 17, 1981 (19811117)
INVENTOR(s): OKUBO MASAO
APPLICANT(s): NIPPON DENSHI ZAIRYO KK [368286] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 55-052655 [JP 8052655]
FILED: April 21, 1980 (19800421)
JOURNAL: Section: P, Section No. 103, Vol. 06, No. 30, Pg. 16, February 23, 1982 (19820223)

ABSTRACT

PURPOSE: To obtain the probe for a high-density **integrated circuit** by arranging an insulating plate whose area is larger than that of an insulating plate wherein a plurality of needles are held over said lower insulating plate, and arranging connecting conductors in the same distribution as the needles.

CONSTITUTION: The first square insulating plate 22 and the second insulating plate 23 whose area is four times that of said insulating plate 22 are arranged so that a specified distance is provided in-between with supporting poles 24. The end of an arm 7 is fixed to the center of the plate 23. A plurality of holes are provided in the corresponding positions at the peripheral parts of the plates 22 and 23. Through said holes, are inserted and fixed pipes 25 comprising thin plates of nickel, stainless steel, and the like. Lead wires 26 comprising fine wires of **gold, copper** , nickel, and the like on which insulation coverings are applied are soldered to the upper ends of the pipes 25 which are protruded from the insulating plate 23. The wires are bundles and extended to each **circuit** of a **printed** board.

08/13/2002 09/813,087

107/3,AB/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04291636
E.I. No: EIP95112931420
Title: Direct production of conductive/resistive traces on a flexible **substrate** using a computer/printer system
Author: Sherman, Paul S.
Corporate Source: Arkansas State Univ, State University, AR, USA
Conference Title: Conference Record of the 1995 IEEE Industry Applications 30th IAS Annual Meeting. Part 2 (of 3)
Conference Location: Orlando, FL, USA Conference Date: 19951008-19951012
E.I. Conference No.: 43982
Source: Conference Record - IAS Annual Meeting (IEEE Industry Applications Society) v 2 1995. IEEE, Piscataway, NJ, USA,95CB35862. p 1817-1821
Publication Year: 1995
CODEN: CIASDZ ISSN: 0197-2618
Language: English
Abstract: Currently, strain gage instrumentation of rocket motor cases involves individually attaching each gage and running lengthy lead wires from the gages to the signal conditioning equipment. The application of many individuals gages is time consuming. Also, the lead wires introduce errors due to their resistance and the electrical noise they absorb. Two areas of interest have been identified which deal with simultaneously applying multiple strain gages and locating the signal conditioning **circuitry** adjacent to the gages. Both of these areas of interest involve the production of conductive and resistive traces on flexible **substrates**. It is desired to produce these traces directly using computer control without having to use a silk screening process or etching of **copper**. The objectives of this study were: 1) Identify technologies which potentially could be developed to produce resistive strain gages and conductive traces for electronic **circuitry** on thin flexible **substrates**. 2) Determine the current capabilities of these technologies as they pertain to the production of conductive and resistive traces. 3) Investigate the technologies to determine the problems which must be overcome in order to produce consistent and reliable results. Although control and timing difficulties present a problem with producing uniform traces, resistances of less than 0.4 Omega /cm (1 Omega /in) were produced with a width of about 1.0 mm (0.04 in). (Author abstract) 30 Refs.

107/3,AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014570854
WPI Acc No: 2002-391558/200242
Related WPI Acc No: 2002-338505
XRPX Acc No: N02-306744
Printhead of **inkjet** printing system, includes several anchor elements which secure ink barrier layer to **substrate** and are encapsulated by **substrate** and ink barrier layer
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: HERNANDEZ J J; TOM D W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6347861	B1	20020219	US 99262872	A	19990302	200242	B

Priority Applications (No Type Date): US 99262872 A 19990302
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6347861	B1		23	B41J-002/05	

Abstract (Basic): US 6347861 B1
Abstract (Basic):
NOVELTY - Several hour-glass shaped metallic anchor elements (252) are positioned on a **substrate** with **fluid** ejector, for securing an ink barrier layer to the **substrate**. The anchor elements are encapsulated by **substrate** and the barrier layer.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) Cartridge;
(b) **Fluid** ejection device
USE - For thermal **inkjet** printing system.
ADVANTAGE - By providing anchor elements, the ink induced shorts, delamination of **printhead** structure, crack propagation, reduced longevity and other problems are avoided.
DESCRIPTION OF DRAWING(S) - The figure shows a cross sectional view of the **printhead**.
Anchor elements (252)
pp; 23 DwgNo 19/20

107/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014416736
WPI Acc No: 2002-237439/200229
Related WPI Acc No: 2002-009264
XRAM Acc No: C02-071825
XRPX Acc No: N02-182708
Article bonding for forming **ink jet printhead**, employs adhesion promoter comprising silane, titanate or zirconate having functional groups including photosensitive aliphatic carbon-carbon double bond linkage(s)
Patent Assignee: XEROX CORP (XERO)
Inventor: DELOUISE L A; LUCA D J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010025690	A1	20011004	US 98105501	A	19980626	200229 B
			US 2001844371	A	20010427	

Priority Applications (No Type Date): US 98105501 A 19980626; US 2001844371 A 20010427
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010025690	A1		45	B32B-031/00	Cont of application US 98105501

Abstract (Basic): US 20010025690 A1
Abstract (Basic):
NOVELTY - Bonding two articles comprises applying an adhesion promoter to polymeric article and/or metal, plasma nitride, silicon, or glass article. The adhesion promoter is silane, titanate or zirconate having (i) alkoxy, aryloxy or arylalkyloxy functional groups and (ii) functional groups including photosensitive aliphatic carbon-carbon double bond linkage(s).

DETAILED DESCRIPTION - Bonding a first article to a second article comprises (a) providing a first article comprising a polymer having photosensitivity-imparting substituents; (b) providing a second article comprising metal, plasma nitride, silicon, or glass; (c) applying an adhesion promoter to the first and/or second article; (d) placing the first article in contact with the second article; and (e) exposing the first article, second article and adhesion promoter to radiation. The adhesion promoter is silane, titanate or zirconate having (i) alkoxy, aryloxy or arylalkyloxy function groups and (ii) functional groups including photosensitive aliphatic C=C linkage(s). INDEPENDENT CLAIMS are also included for (A) an **ink jet printhead** comprising (i) an upper **substrate** (31) with a set of parallel grooves for subsequent use as ink channels and a recess for subsequent use as a manifold; (ii) a lower **substrate** with one surface having an array of heaters and addressing **electrodes** (33) and comprising metal, plasma nitride, silicon, or glass; and (iii) an insulative layer (18) deposited on surface of lower **substrate** and over heaters and

electrodes and patterned to form recesses to expose heaters and **electrode** terminals (32); and (B) a process for forming an **ink jet printhead** by providing a lower **substrate**; depositing an adhesion promoter onto the surface of the lower **substrate**; depositing an insulative layer comprising a polymer having photosensitivity-imparting substituents; exposing the adhesion promoter and the insulative layer to actinic radiation in an imagewise pattern such that the polymer in exposed areas becomes crosslinked or chain extended and the polymer in unexposed areas corresponding to areas of the lower **substrate** having the heaters and terminal ends of **electrodes** is not crosslinked or chain extended; removing the adhesion promoter and the polymer from the unexposed areas to form recesses in the layer; providing an upper **substrate** with a set of parallel grooves which are open at one end for serving as droplet emitting nozzles (27); and aligning, mating, and bonding the upper and lower **substrates** together to form a **printhead** where the grooves in the upper **substrate** are aligned with the heaters in the lower **substrate**.

USE - For forming an **ink jet printhead**.

ADVANTAGE - The adhesion promoter enables good interfacial adhesion of photopolymer films on plasma nitride, metal, silicon, or glass surfaces. It also enables the formation of protective layers and **fluid paths** in **ink jet printheads** that are highly resistant to hydrolysis degradation. The adhesion promoter in photopatternable articles provides good layer adhesion during the development process. Undercutting and floating images are reduced or eliminated.

DESCRIPTION OF DRAWING(S) - The figure shows an enlarged schematic isometric view of a **printhead** mounted on a daughter board showing the droplet emitting nozzles.

Insulative layer (18)
Droplet emitting nozzles (27)
Upper **substrate** (31)
Electrode terminals (32)
Addressing **electrodes** (33)

107/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013167707
WPI Acc No: 2000-339580/200029
XRAM Acc No: C00-103042
XRPX Acc No: N00-254952
Inkjet printhead for **inkjet** printers has a series of nozzles for the ejection of ink, each nozzle having a rim formed by the deposition of a rim material layer over a sacrificial layer and subsequent planar removal of the rim layer
Patent Assignee: SILVERBROOK RES PTY LTD (SILV-N); SILVERBROOK K (SILV-I)
Inventor: SILVERBROOK K
Number of Countries: 091 Number of Patents: 012
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200023279	A1	20000427	WO 99AU894	A	19991015	200029	B
US 6273544	B1	20010814	US 99425419	A	19991019	200148	

Priority Applications (No Type Date): AU 987023 A 19981109; AU 986534 A 19981016; AU 986535 A 19981016; AU 986536 A 19981016; AU 986537 A 19981016; AU 986538 A 19981016; AU 986539 A 19981016; AU 986540 A
US 6273544 B1 B41J-002/01

Abstract (Basic): WO 200023279 A1
Abstract (Basic):
NOVELTY - An **inkjet printhead** has a series of nozzles for the ejection of ink. Each nozzle has a rim formed by the deposition of a rim material layer (42) over a sacrificial layer (41) and subsequent planar removal of the rim layer to form the nozzle rim.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(A) A method of forming an **inkjet printhead** on a **substrate**, comprising:
(a) providing a first **substrate** where electrical drive **circuitry** made up of layers of conductive, semi-conductive and non-conductive materials is formed, for the control of **inkjet printhead**; and
(b) forming on the **substrate** a nozzle chamber with ink ejection aperture in a wall and ink external thermal actuator to eject ink from the aperture, where portions of one of the **substrate**'s layers are utilized as a sacrificial material layer in the formation of ink actuator. (B) A method of operation of a **fluid** ejection **printhead** within a predetermined thermal range so as to print an image, comprising:
(a) sensing the **printhead** temperature to determine if it is below a predetermined threshold;
(b) preheating the **printhead** is temperature is below the threshold;
(c) controlling the preheating such that thermal actuators are heated to an extent insufficient to eject **fluid** from the **printhead**; and
(d) utilizing the **printhead** to print the image.

(C) A **fluid** ejection device comprising an array of nozzles formed on a **substrate** and adapted to eject ink on demand using the ink actuators, a temperature sensor attached to **substrate**, and a temperature sensor unit.

(D) An ink supply arrangement for supplying ink to the printing arrangement of a portable printer, including an ink supply unit with a storage chamber for holding ink and a series of spaced apart baffles to reduce the acceleration of the ink within the unit as may be induced by movement of the printer while allowing for flows of ink to the printing arrangement in response to active demand.

(E) A power distribution arrangement for an elongate **inkjet printhead** with spaced voltage supply points, including two or more elongate low resistance power supply busbars, and tape automated bonded (TAB) film to connect selected supply points to the busbars.

(F) An ink supply unit for supplying a **printhead** containing an array of ink ejection nozzles, comprising baffles having a cavity and/or in the form of ink distribution manifold with a second cavity for the insertion of **printhead**.

(G) A method of interconnecting a **printhead** to an ink distribution manifold, comprising attaching the **printhead** to the manifold using a resilient adhesive to be elastically deformed with any deflections of the manifold.

(H) A **printhead** and ink distribution manifold assembly. (I) A method of improving the operational characteristics of the **printhead** comprising locating an end portion on the movable paddle, the portion moving towards the nozzle aperture upon activation of the liquid ejection paddle to eject the **fluid**.

(J) An **inkjet printhead** apparatus comprising nozzle chambers, ink supply channel interconnected with the chamber, paddle and an end portion interconnecting the paddle's portion.

USE - For **inkjet** printers.

ADVANTAGE - The **printhead** has high resolution which allows full photographic quality color images and high quality text. It allows high-speed operation, as no scanning is required. It is inexpensive and compact because as the nozzle density of the **printhead** is very high, the chip area per **print head** can be low, thus allowing multiple head designs. The **printhead**'s high resolution allows a fully digital operation using digital half toning which eliminates color non-linearity. The **printhead** has small drop volume and accurate control of drop velocity. It allows fast drying and eliminates paper cockle. It has a wide temperature range and requires no special manufacturing equipment in moving from laboratory to production. It has high production capacity available, provides low factory setup cost, good light-fastness, good water-fastness, excellent color gamut, eliminates color bleed and has high nozzle count. No precision assembly is required because the **printhead** is made as a single monolithic CMOS chip. The **printhead** allows duplex printing at full print speed and is more efficient. It generates low pressure, requires low power, operates at low voltage and has low power consumption that a photographic **printhead** can operate from AA batteries. Manufacturing process is less complex and packaging is of low cost. The **printhead** has no thermal, fluidic or structural crosstalk, no cavitation or electromigration. It has reliable power connections and has no corrosion, electrolysis, fatigue, friction,

107/3,AB/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010270357
WPI Acc No: 1995-171612/199523
Related WPI Acc No: 1997-315602
XRPX Acc No: N95-134507
Bubble **ink-jet** printer - uses heating action of thin film thermal resistor to heat **fluid** with bubbles used to expel ink from nozzles
Patent Assignee: HITACHI KOKI KK (HITO)
Inventor: MACHIDA O; MITANI M; SHIMIZU K; YAMADA K; KAWASUMI K
Number of Countries: 002 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4438936	A1	19950504	DE 4438936	A	19941031	199523	B
US 5729260	A	19980317	US 94331742	A	19941031	199818	
DE 4438936	C2	19980610	DE 4438936	A	19941031	199827	
US 5980024	A	19991109	US 94331742	A	19941031	199954	
			US 96740895	A	19961104		

Priority Applications (No Type Date): JP 93272451 A 19931029; JP 95285650 A 19951102
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4438936	A1		13	B41J-002/05	
US 5729260	A		11	B41J-029/38	
US 5980024	A			B41J-002/05	CIP of application US 94331742
					CIP of patent US 5729260
DE 4438936	C2			B41J-002/05	

Abstract (Basic): DE 4438936 A
The bubble **ink jet** printer uses a thermal effect to generate output from the nozzles. The **print head** has a thin film resistor (3) formed on the surface of a silicon **substrate** (1). The resistor is produced of a Cr.Si.SiO alloy and has an associated **integrated circuit** as a drive stage.
An alternative stage is of **Ta**.Si.SiO alloy. The thermal resistance exhibits a fast response heating cycle with ink being expelled from the nozzles due to the change in bubbles formed in the **fluid**.
ADVANTAGE - Stable operation. Increased **ink jet** frequency.
Dwg.4/7
Abstract (Equivalent): US 5729260 A
The bubble **ink jet** printer uses a thermal effect to generate output from the nozzles. The **print head** has a thin film resistor (3) formed on the surface of a silicon **substrate** (1). The resistor is produced of a Cr.Si.SiO alloy and has an associated **integrated circuit** as a drive stage.
An alternative stage is of **Ta**.Si.SiO alloy. The thermal resistance exhibits a fast response heating cycle with ink being

expelled from the nozzles due to the change in bubbles formed in the **fluid.**

ADVANTAGE - Stable operation. Increased **ink jet** frequency.

Dwg.6/7

107/3,AB/6 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009984635
WPI Acc No: 1994-252346/199431
XRPX Acc No: N94-199259
Fluid support ion projection **print head** for electrostatic image recorder e.g. printer - has main part with slit-like ion control discharge mouth, and positioning notch at each end of **substrate** with control **electrode**, with ion discharge modulated by image signal
Patent Assignee: FUJI XEROX CO LTD (XERF)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6183053	A	19940705	JP 92356511	A	19921222	199431	B

Priority Applications (No Type Date): JP 92356511 A 19921222
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6183053	A		6	B41J-002/415	

Abstract (Basic): JP 6183053 A

The **print head** consists of a side board (4) fixed at both ends of a head main part (1). An ion abnormal conditions device (3) consists of an ion generator (2) and a **substrate** (9) with control and opposite **electrode** board (10). This forms an ion control discharge mouth (13) and the head main part. A notch (16) is formed at each end of the **substrate**, and a protrusion (18) is contacted to an electrostatic image holder. Each part constituting the ion generator and the ion abnormal conditions device has an exact relative position.

The head main part supplies **fluid** for ion conveyance by connecting to an ion generator movable longitudinally. The **print head** makes an electrostatic latent image form **w**.r.t. the picture signal from the ion style control discharge mouth.

USE/ADVANTAGE - For copier, facsimile etc. High resolution image. Simpler attachment fixation. Constant clearance between **print head** and electrostatic latent image holder.

Dwg.1/5

107/3,AB/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

004339394
WPI Acc No: 1985-166272/198528
XRAM Acc No: C85-072691
XRPX Acc No: N85-125181
Ink jet print head - has electrothermal stage **electrodes** protected by insulating layers with good adhesion and corrosion resistance
Patent Assignee: CANON KK (CANO)
Inventor: IKEDA M; KOMURO H; MATSUDA H; SHIBATA M; TAKAHASHI H; TSUDA H
Number of Countries: 004 Number of Patents: 013
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5455612	A	19951003	US 84684114	A	19841220	199545
			US 8729370	A	19870324	

Priority Applications (No Type Date): JP 8414518 A 19840131; JP 83249079 A 19831226
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
					Div ex patent DE 3446968
US 5455612	A		16	B41J-002/05	Cont of application US 84684114
					Cont of application US 8729370

Abstract (Basic): DE 3446968 A

The **ink jet print head** (100) has an opening (104) and exit section for the droplets (105) and an electro thermal converter (101) with a **substrate** (102) and a top plate (103) with grooves that provide a line density. The heat generating section (107) operates on a specific section (106) with a surface (108) in contact with the liq..

The heat generating section has a base (115) and sepg. layer (109) that supports a resistive film (110) with an insulating layer (111) containing **electrodes** (113, 114). The latter are protected from the **fluid** by the insulating layer (111) which is produced from an inorganic oxide, e.g. SiO2 and an inorganic nitride, e.g. Si3.N4. A second protective layer (116) has good adhesion and corrosion resistant properties, such as **Ta**.

ADVANTAGE - Improved operational life of electrothermal converter.

1H/5

Abstract (Equivalent): DE 3446968 C

A liq. jet writing head includes at least one liq. channel with a resistance heater and **electrodes**, where the resistance heater between the **electrodes** forms an electrothermal transducer, a primary protection layer comprising an inorganic insulating material and sec. and tert. insulation layers. The overlapping width between the sec. protective layer and the tert. protective layer is 10-500 microns. The prim. protective layer pref. consists of a transition metal oxide, while the tert. protective layer consists of a light sensitive polyimide resin.

ADVANTAGE - The head is reliable and can be used many times. (10pp)
DE 3448367 C

Liq. beam recording head comprises a **substrate** having a resistance heating layer and **electrode** electrically connected to the resistance layer. The resistance layer forms an electrothermal converter. The head also has an upper layer having a 1st. protective layer made of an inorganic insulation material and a 2nd. protective layer made of an organic material. The 2nd. protective layer (116) is arranged on the 1st. protective layer (111).

ADVANTAGE - High quality head is produced.
Dwg.2/2

Abstract (Equivalent): GB 2153304 B

A **liquid jet** recording head having: a **substrate** comprising: a support, a resistive heater layer, **electrodes** electrically connected with the resistive heater layer, a portion of the resistive heater layer located between the **electrodes** providing an electrothermal transducer; and an upper layer comprising: a first protective layer comprising an inorganic insulating material; a second protective layer comprising an inorganic material, and athird protective layer comprising an organic material; a liquid flow **path** being provided on the **substrate** and corresponding to the electrothermal transducer; the upper layer having: a region where the first protective layer overlies the electrothermal transducer and the second protective layer overlies said first protective layer, and other regions, adjacent the electrothermal transducer, where the first protective layer overlies the **electrodes** under the liquid flow **path**, and where the third protective layer overlies the first protecting layer, wherein the second protective layer extends from the first region overlying the electrothermal transducer portion into the other regions, and the second and third protective layers overlap each other in each of the other regions with an overlap in the range from 10 to 500 micrometers.

GB 2188004 B

A **liquid jet** recording head having a **substrate** and an upper layer; the **substrate** having a support, a resistive heater layer and **electrodes** electrically connected with the resistive heater layer such that portions of the resistive heater layer located between the **electrodes** provide a plurality of electrothermal transducers for heating recording liquid; the upper layer comprising a first protective layer comprising an inorganic insulating material, and a second protective layer comprising an inorganic material; the first and second protective layers being successively formed at least on the electrothermal transducers and the second protective layer being in the form of a continuous strip which covers adjacent electrothermal transducers.

109/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013586723
WPI Acc No: 2001-070930/200108
XRAM Acc No: C01-019776
XRPX Acc No: N01-053695
Ink-jet printer head for, e.g., thermal **ink-jet** printer, includes an ink-corrosion resistant barrier layer which covers a pair of **electrodes**, so that the **electrodes** are not exposed to the ink in the ink flow passage
Patent Assignee: CASIO COMPUTER CO LTD (CASK)
Inventor: KAMADA H
Number of Countries: 015 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6350017	B1	20020226	US 2000580644	A	20000530	200220

Priority Applications (No Type Date): JP 99151322 A 19990531
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6350017	B1			B41J-002/05	

Abstract (Basic): WO 200073077 A1
Abstract (Basic):
NOVELTY - An **ink-jet** printer head includes a barrier layer (41) which is ink-corrosion resistant. The barrier layer covers a pair of **electrodes**, so that the **electrodes** are not exposed to the ink in the ink flow passage.
DETAILED DESCRIPTION - An **ink-jet** printer head in which ink is pressed out in predetermined directions by vapor bubbles generated by heating the ink, comprises: an insulation **substrate** (18, 19) having insulating surface(s); heating resistors (24) formed on the **substrate**, each having a heating area (25) which emits heat when a predetermined voltage is applied to it; a pair of **electrodes** (21, 23) electrically connected to each heating area; a wall (11) formed on the **substrate** to determine an ink flow passage; and a barrier layer having an ink-corrosion resistance. The barrier layer covers the **electrodes** so that they are not exposed to the ink in the ink flow passage.
INDEPENDENT CLAIMS are also included for the following:
(a) an **ink-jet** printer head which includes pressure generators which provide pressure to the ink when a predetermined voltage is applied, **electrodes**, and the above barrier layer. The ink is pressed out through nozzles in predetermined **directions** by providing **pressure** to the ink; and
(b) a manufacturing method of the above **ink-jet** printer head.
Preferred Features: The **ink-jet printhead** further comprises a contact layer (39) formed between the **electrodes** and the heating resistors; and a protective insulation film formed over the heating areas and the barrier layer.
USE - The **ink-jet** printer head is used for thermal

ink-jet printer or **ink-jet** printer which generates pressure energy to output ink, or non-monolithic **ink-jet** printer in which the drive **circuits** are separated from a head **substrate**.

ADVANTAGE - The **ink-jet** printer head has a resistance against corrosion and migration caused by ink, thus reliability is improved.

DESCRIPTION OF DRAWING(S) - The figure is a cross sectional view schematically showing the structure of a heating element in the **ink-jet** printer head.

Wall (11)
Insulation **substrates** (18, 19)
Electrodes (21, 23)
Heating resistors (24)
Heating area (25)
Contact layer (39)
Barrier layer (41)